CeraLink

Capacitor for fast-switching semiconductors

Series/Type: Low profile (LP) series
Ordering code: B58031*
Date: 2023-03-30
Version: 6.2
Applications
- Power converters and inverters
- DC link/snubber capacitor for power converters and inverters

Features
- High ripple current capability
- High temperature robustness
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several MHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- Qualification based on AEC-Q200 rev. D
- Suitable for reflow soldering only

Construction
- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper-invar leadframe
- Epoxy resin adhesive

General technical data

<table>
<thead>
<tr>
<th></th>
<th>tan δ</th>
<th>Insulation resistance $R_{\text{ins, typ}}$</th>
<th>Operating device temperature $T_{\text{device}}$</th>
<th>Weight of device</th>
<th>Dissipation factor</th>
<th>Insulation resistance $R_{\text{ins, typ}}$</th>
<th>Operating device temperature $T_{\text{device}}$</th>
<th>Weight of device</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt; 0.02</td>
<td>&gt; 1</td>
<td>-40 °C to +150 °C</td>
<td>approx. 1.3 g</td>
<td>tan δ</td>
<td>&gt; 1</td>
<td>-40 °C to +150 °C</td>
<td>approx. 1.3 g</td>
</tr>
</tbody>
</table>

1) Typical insulation resistance, measured at operating voltage $V_{\text{op}}$ and measurement time > 240 s, +25 °C
Electrical specifications and ordering codes

<table>
<thead>
<tr>
<th>Lead type</th>
<th>V_{pk, max} V</th>
<th>V_{R, Tmax} (^1)</th>
<th>V_{op} V</th>
<th>C_{nom, typ} (\mu F)</th>
<th>C_{eff, typ} (\mu F)</th>
<th>C_0 (\mu F)</th>
<th>Ordering code</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-style</td>
<td>650</td>
<td>500</td>
<td>400</td>
<td>1</td>
<td>0.6</td>
<td>0.35 ±20%</td>
<td>B58031I5105M062</td>
</tr>
<tr>
<td>J-style</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>B58031U5105M062</td>
</tr>
<tr>
<td>L-style</td>
<td>1000</td>
<td>700</td>
<td>600</td>
<td>0.5</td>
<td>0.25</td>
<td>0.14 ±20%</td>
<td>B58031I7504M062</td>
</tr>
<tr>
<td>J-style</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>B58031U7504M062</td>
</tr>
<tr>
<td>L-style</td>
<td>1300</td>
<td>900</td>
<td>800</td>
<td>0.25</td>
<td>0.13</td>
<td>0.07 ±20%</td>
<td>B58031I9254M062</td>
</tr>
<tr>
<td>J-style</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>B58031U9254M062</td>
</tr>
</tbody>
</table>

\(^1\)V_{R, Tmax} denotes the permissible rated voltage for the maximum device temperature T_{max} = +150 °C. Operation at higher rated voltage \(V_R > V_{R, Tmax}\) is possible. The permissible rated voltage \(V_R\) can be taken from the temperature derating curves on the next page.

Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time. The typical aging rate is about 2.5% per logarithmic decade in hours.
Rated voltage $V_R$ and temperature derating

The CeraLink LP series can be operated at elevated rated voltage, i.e. $V_R \geq V_{R, \text{Tmax}}$. However, the device temperature of the component should be kept within the temperature-derated conditions detailed in the following figures. Higher device temperatures are permissible at reduced lifetime.

- $V_{R, \text{Tmax}} = 500$ V (B58031*5*)
- $V_{R, \text{Tmax}} = 700$ V (B58031*7*)
- $V_{R, \text{Tmax}} = 900$ V (B58031*9*)
CeraLink B58031*
Capacitor for fast-switching semiconductors Low profile (LP) series

Dimensional drawings

L-style

![L-style diagram](image1)

Dimensions in mm

J-style

![J-style diagram](image2)

Dimensions in mm

Recommended solder pads

![Solder pads diagram](image3)

Dimensions in mm

![Solder pads diagram](image4)

Dimensions in mm
Polarity and marking of components

L-style

J-style

Manufacturer’s logo
CeraLink type
X.XX = Nominal capacitance (1, 0.5, 0.25)
YYY = Rated voltage (500, 700, 900)

Note that polarity is only for incoming inspection purposes and it does not affect operation. If put under reverse rated voltage \( V_R \), CeraLink is repoled and works identically, see our CeraLink Technical Guide for further details.

Typical values as a design reference for CeraLink applications

<table>
<thead>
<tr>
<th>( V_R, T_{\text{max}} )</th>
<th>ESR ( 0 \text{ V DC}, 0.5 \text{ V AC (RMS)}, 25 \degree \text{C}, 1 \text{ kHz} )</th>
<th>ESR ( 0 \text{ V DC}, 0.5 \text{ V AC (RMS)}, 25 \degree \text{C}, 1 \text{ MHz} )</th>
<th>ESL</th>
<th>( I_{\text{op}^*} )</th>
<th>( I_{\text{op}^*} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( \text{m\Omega} )</td>
<td>( \text{m\Omega} )</td>
<td>( \text{nH} )</td>
<td>( V_{\text{op}} )</td>
<td>100 kHz</td>
</tr>
<tr>
<td>500</td>
<td>3</td>
<td>12</td>
<td>3</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>700</td>
<td>6</td>
<td>24</td>
<td>3</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>900</td>
<td>14</td>
<td>45</td>
<td>3</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

\(^*\) Normal operating current without forced cooling at \( T_{\text{device}} = +150 \degree \text{C} \). Higher values permissible at reduced lifetime.
Application notes

Further typical electrical characteristics as a design reference for CeraLink applications.

Typical characteristics as a function of temperature and voltage - $V_R, T_{max} = 500$ V
(0.5 V AC (RMS), frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to $\tan \delta$, $C_{eff, typ}$ and ESR$_{1kHz}$ which are given on page 2, 3 and 6 of this data sheet.
**Typical capacitance values as a function of voltage - $V_{R, \text{T}_{\text{max}}} = 500 \, \text{V}$**

**Large signal capacitance:**
Quasistatic (slow variation of the voltage), $+25 \, ^\circ\text{C}$.
The nominal capacitance is defined as the large signal capacitance at $V_{\text{op}}$.
See glossary for further information.

**Small signal capacitance:**
0.5 V AC (RMS), 1 kHz, $+25 \, ^\circ\text{C}$
The effective capacitance is defined as the small signal capacitance at $V_{\text{op}}$.

**Typical impedance and ESR as a function of frequency - $V_{R, \text{T}_{\text{max}}} = 500 \, \text{V}$**

0 V DC, 0.5 V AC (RMS), $T_{\text{device}} = 25 \, ^\circ\text{C}$

**Typical permissible current as a function of frequency - $V_{R, \text{T}_{\text{max}}} = 500 \, \text{V}$**

Measurement performed at $V_{\text{op}}$.
The values correspond to a device temperature of $+150 \, ^\circ\text{C}$.
No forced cooling was used.
Note that with additional cooling the typical permissible current can be significantly higher.
Typical characteristics as a function of temperature and voltage - \( V_R, T_{max} = 700 \, V \)
(0.5 V AC (RMS), frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to \( \tan \delta, C_{eff, \, typ} \) and \( ESR_{1kHz} \) which are given on page 2, 3 and 6 of this data sheet.
Typical capacitance values as a function of voltage - \( V_R, T_{\text{max}} = 700 \text{ V} \)

- **Large signal capacitance:**
  - Quasistatic (slow variation of the voltage), +25 °C.
  - The nominal capacitance is defined as the large signal capacitance at \( V_{\text{op}} \).
  - See glossary for further information.

- **Small signal capacitance:**
  - 0.5 V AC (RMS), 1 kHz, +25 °C
  - The effective capacitance is defined as the small signal capacitance at \( V_{\text{op}} \).

Typical impedance and ESR as a function of frequency - \( V_R, T_{\text{max}} = 700 \text{ V} \)

- 0 V DC, 0.5 V AC (RMS), \( T_{\text{device}} = 25 \text{ °C} \)

Typical permissible current as a function of frequency - \( V_R, T_{\text{max}} = 700 \text{ V} \)

- Measurement performed at \( V_{\text{op}} \).
- The values correspond to a device temperature of 150 °C.
- No forced cooling was used.
- Note that with additional cooling the typical permissible current can be significantly higher.
Typical characteristics as a function of temperature and voltage - $V_R$, $T_{max} = 900$ V
(0.5 V AC (RMS), frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to $\tan \delta$, $C_{eff,\,typ}$ and $ESR_{1kHz}$ which are given on page 2, 3 and 6 of this data sheet.
Typical capacitance values as a function of voltage - $V_R, T_{\text{max}} = 900 \text{ V}$

**Large signal capacitance:**
Quasistatic (slow variation of the voltage), $+25 \degree \text{C}$.
The nominal capacitance is defined as the large signal capacitance at $V_{\text{op}}$.
See glossary for further information.

**Small signal capacitance:**
0.5 V AC (RMS), 1 kHz, $+25 \degree \text{C}$
The effective capacitance is defined as the small signal capacitance at $V_{\text{op}}$.

Typical impedance and ESR as a function of frequency - $V_R, T_{\text{max}} = 900 \text{ V}$

0 V DC, 0.5 V AC (RMS), $T_{\text{device}} = 25 \degree \text{C}$

Typical permissible current as a function of frequency - $V_R, T_{\text{max}} = 900 \text{ V}$

Measurement performed at $V_{\text{op}}$.
The values correspond to a device temperature of 150 °C.
No forced cooling was used.
Note that with additional cooling the typical permissible current can be significantly higher.
Reliability

A. Preconditioning
■ Solder the capacitor on a PCB using the recommended soldering profile
■ Check of external appearance
■ Measurement of isolation resistance $R_{\text{ins}}$:
  - Apply $V_{\text{pk, max}}$ for 7 seconds and measure $R_{\text{ins}}$ at room temperature:
    - Isolation resistance ($@ V_{\text{pk, max}}, 7$ s, $25$ °C) $R_{\text{ins}} > 100$ MΩ
■ Measurement of electrical parameters $C_0$ and $\tan \delta$ according to specification:
  - Measure $C_0$ and $\tan \delta$ within 10 minutes to 1 hour afterwards:
    - Initial capacitance ($@ 0$ V DC, $0.5$ V AC (RMS), $1$ kHz, $25$ °C) $C_0$ acc. spec. on page 3
    - Dissipation factor ($@ 0$ V DC, $0.5$ V AC (RMS), $1$ kHz, $25$ °C) $\tan \delta < 0.02$

B. Performance of a specific reliability test

C. After performing a specific test
■ Check the external appearance again
■ Repeat the measurement of the electrical parameters:
  - Apply $V_{\text{pk, max}}$ for 7 seconds and measure $R_{\text{ins}}$ at room temperature:
    - Isolation resistance ($@ V_{\text{pk, max}}, 7$ s, $25$ °C) $R_{\text{ins}} > 100$ MΩ
  - Measure $C_0$ and $\tan \delta$:
    - Change of initial capacitance ($@ 0$ V DC, $0.5$ V AC (RMS), $1$ kHz, $25$ °C) $|\Delta C_0/C_0| < 15\%$
    - Dissipation factor ($@ 0$ V DC, $0.5$ V AC (RMS), $1$ kHz, $25$ °C) $\tan \delta < 0.05$

*) Note that the measurement of the isolation resistance $R_{\text{ins}}$ using the described measurement conditions is for pre- and post-measurement within the scope of the AEC-Q200 reliability tests only.

Qualification tests based on AEC-Q200 Rev. D (Table 2)

<table>
<thead>
<tr>
<th>Test</th>
<th>No</th>
<th>Standard</th>
<th>Test conditions</th>
<th>Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre- and post-stress electrical</td>
<td>1</td>
<td>-</td>
<td>As described above</td>
<td>$</td>
</tr>
<tr>
<td>High temperature exposure</td>
<td>3</td>
<td>MIL-STD-202 Method 108</td>
<td>$+150$ °C, unpowered, 1000 hours</td>
<td>No mechanical damage $</td>
</tr>
<tr>
<td>Temperature cycling</td>
<td>4</td>
<td>JESD22 Method JA-104</td>
<td>$-55$ °C to $+150$ °C, $\leq 20$ seconds transfer time, $15$ minutes dwell time, $1000$ cycles</td>
<td>No mechanical damage $</td>
</tr>
<tr>
<td>Destructive physical analysis</td>
<td>5</td>
<td>EIA-469</td>
<td>-</td>
<td>No internal defects that might affect performance or reliability</td>
</tr>
<tr>
<td>Biased humidity</td>
<td>7</td>
<td>MIL-STD-202 Method 103</td>
<td>$+85$ °C, 85% rel. hum., $V_R$, $T_{\text{max}}$, $1000$ hours</td>
<td>No mechanical damage $</td>
</tr>
<tr>
<td>High temperature operating life</td>
<td>8</td>
<td>MIL-STD-202 Method 108</td>
<td>$+150$ °C, $V_R$, $T_{\text{max}}$, $1000$ hours</td>
<td>No mechanical damage $</td>
</tr>
<tr>
<td>External visual</td>
<td>9</td>
<td>MIL-STD-883 Method 2009</td>
<td>Visual inspection with magnifying glass</td>
<td>No defects that might affect performance</td>
</tr>
</tbody>
</table>
# CeraLink B58031*

**Capacitor for fast-switching semiconductors**

**Low profile (LP) series**

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## Test Conditions

<table>
<thead>
<tr>
<th>Test</th>
<th>No.</th>
<th>Standard</th>
<th>Test conditions</th>
<th>Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical dimension</td>
<td>10</td>
<td>JESD22 Method JB-100</td>
<td>Verify physical dimensions to the device specification using a caliper and a gauge</td>
<td>Within specified values in the chapter dimensional drawing</td>
</tr>
<tr>
<td>Tensile strength (unsoldered)</td>
<td>11</td>
<td>MIL-STD-202 Method 211</td>
<td>Apply a force of 10 N in the shown direction. Ceramic body is clamped:</td>
<td>No detaching of termination. $</td>
</tr>
<tr>
<td>Resistance to solvent</td>
<td>12</td>
<td>MIL-STD-202 Method 215</td>
<td>Dipping and cleaning with isopropanol</td>
<td>Marking must be legible $</td>
</tr>
<tr>
<td>Mechanical shock</td>
<td>13</td>
<td>MIL-STD-202 Method 213</td>
<td>Acceleration 400 m/s². Half sine pulse duration 6 milliseconds 4000 bumps</td>
<td>No mechanical damage $</td>
</tr>
<tr>
<td>Vibration</td>
<td>14</td>
<td>MIL-STD-202 Method 204</td>
<td>5 g / 20 min. 12 cycles, 3 axes 10 Hz to 2000 Hz</td>
<td>No mechanical damage $</td>
</tr>
<tr>
<td>Resistance to soldering heat</td>
<td>15</td>
<td>MIL-STD-202 Method 210 Condition B</td>
<td>Dip test of contact areas in solder bath (+260 °C for 10 seconds)</td>
<td>No damage of pin silver coating, $</td>
</tr>
<tr>
<td>Solderability</td>
<td>18</td>
<td>See below</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Board flex</td>
<td>21</td>
<td>AEC-Q200-005</td>
<td>Bending of 2 mm for 60 seconds</td>
<td>No mechanical damage. $</td>
</tr>
<tr>
<td>Terminal strength</td>
<td>22</td>
<td>AEC-Q200-006</td>
<td>Apply a force of 17.7 N for 60 seconds</td>
<td>No detaching of termination. No rupture of ceramic. $</td>
</tr>
</tbody>
</table>

### Solderability Tests

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Wettability (leadframe only)</td>
<td>J-STD-002, Method A @ 235 °C, cat. 3</td>
<td>Dipping of contact areas in solder bath (+235 °C for 5 seconds)</td>
<td>&gt; 95% wettability of lead frame</td>
</tr>
<tr>
<td>Leaching test (leadframe only)</td>
<td>MIL-STD-202, Method 210, cond. B</td>
<td>Dipping of contact areas in solder bath (+260 °C for 10 seconds)</td>
<td>No damage of lead frame silver coating</td>
</tr>
<tr>
<td>Reflow test</td>
<td>-</td>
<td>3 times recommended reflow soldering profile</td>
<td>No mechanical damage. Proper solder coating of contact areas. $</td>
</tr>
</tbody>
</table>
Packaging

The CeraLink LP types are delivered in a blister tape (taping to IEC 60286-3).

Blister tape for L-style terminal

Blister tape for J-style terminal

Part orientation for L-style terminal

Part orientation for J-style terminal
Taping information

Trailer: There is a minimum of 160 mm of carrier tape with empty compartments and sealed by the cover tape.

Leader: There is a minimum of 400 mm of cover tape, which includes at least 100 mm of carrier tape with empty compartments.

Fixing peeling strength (top tape)

The peeling strength is 0.1 … 1.3 N.
Reel packing

<table>
<thead>
<tr>
<th></th>
<th>L-style terminal 330-mm reel</th>
<th>J-style terminal 330-mm reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>330 ±2</td>
<td>330 ±2</td>
</tr>
<tr>
<td>B</td>
<td>100 ±1</td>
<td>62 ±1</td>
</tr>
<tr>
<td>C</td>
<td>13 +0.5/-0.2</td>
<td>12.8 ±0.7</td>
</tr>
<tr>
<td>D</td>
<td>20.2 min.</td>
<td>19.1 min.</td>
</tr>
<tr>
<td>E</td>
<td>2.2 ±0.2</td>
<td>1.6 ±0.5</td>
</tr>
<tr>
<td>W</td>
<td>24.2 +2</td>
<td>16.4 +2</td>
</tr>
</tbody>
</table>

Dimensions in mm
Recommended reflow soldering profile

<table>
<thead>
<tr>
<th>Profile feature</th>
<th>SAC, Sn95.5Ag3.8Cu0.7 @ N₂ atmosphere</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preheat and soak</td>
<td></td>
</tr>
<tr>
<td>- Temperature min</td>
<td>( T_{\text{min}} )</td>
</tr>
<tr>
<td>- Temperature max</td>
<td>( T_{\text{max}} )</td>
</tr>
<tr>
<td>- Time ( t_{\text{min}} ) to ( t_{\text{max}} )</td>
<td>60 … 120 seconds</td>
</tr>
<tr>
<td>Average ramp-up rate</td>
<td>( T_{L} ) to ( T_{P} )</td>
</tr>
<tr>
<td>Liquidus temperature</td>
<td>( T_{L} )</td>
</tr>
<tr>
<td>Time at liquidus temperature</td>
<td>( t_{L} )</td>
</tr>
<tr>
<td>Peak package body temperature</td>
<td>( T_{P} )</td>
</tr>
<tr>
<td>Time ( (t_{P}) ) within +5 °C of specified classification temperature ( (T_{c}) )</td>
<td>30 seconds (^{3)})</td>
</tr>
<tr>
<td>Average ramp-down rate</td>
<td>( T_{P} ) to ( T_{L} )</td>
</tr>
<tr>
<td>Time +25 °C to peak temperature</td>
<td>maximum 8 minutes</td>
</tr>
</tbody>
</table>

1) Tolerance for peak profile temperature \( (T_{P}) \) is defined as a supplier minimum and a user maximum.
2) Depending on package thickness (cf. JEDEC J-STD-020D).
3) Tolerance for time at peak profile temperature \( (t_{P}) \) is defined as a supplier minimum and a user maximum.

Notes:
- All temperatures refer to topside of the package, measured on the package body surface.
- Max. number of reflow cycles: 3
- After the soldering process, the capacitance is lowered. Applying \( V_R \) to the device will re-establish the capacitance.
- The proposed soldering profile is based on IEC 60068-2-58 (respectively JEDEC J-STD-020D) recommendations.
CeraLink B58031*
Capacitor for fast-switching semiconductors Low profile (LP) series

General technical information

Storage
- Only store CeraLink capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature −25 °C to +45 °C, relative humidity ≤ 75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink capacitors where they are exposed to heat or direct sunlight. Otherwise, the packaging material may be deformed or CeraLink may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink surface during storage, handling and processing.
- Avoid storing CeraLink devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraLink components within 12 months after shipment.

Handling
- Do not drop CeraLink components or allow them to be chipped.
- Do not clamp CeraLink components on the face sides (e.g. during pick-and-place). A vacuum-based pick-and-place process picking the component on the top side is recommended.
- Do not touch CeraLink with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink surface during handling.
- The CeraLink LP series was tested to withstand the board flex test defined in the AEC-Q200 rev D, method 005.
- The CeraLink LP series uses copper-invar lead frames to prevent mechanical stress to the ceramic. Too much bending causes open mode. Avoid high mechanical stress like twisting after soldering on a PCB.
Mounting
- Do not subject CeraLink devices to mechanical stress when encapsulating them with sealing material or overmolding with plastic material. Encapsulation may also lead to worse heat dissipation. Please ask for further information.
- Do not scratch the electrodes before, during, or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink components are clean before mounting.
- The surface temperature of an operating CeraLink can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink to allow proper cooling.
- Avoid contamination of the CeraLink surface during processing.

Soldering guidelines
- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an unstable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.

- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink may cause damage to the component.
- Excessive washing like ultrasonic cleaning, can affect the connection between the ceramic chip and the outer electrode. To avoid this, we give the following recommendation:
  - Power: 20 W/I max.
  - Frequency: 40 kHz max.
  - Washing time: 5 minutes max.
Glossary

- **Initial capacitance** $C_0$: Is the value at the origin of the hysteresis without any applied direct voltage.

- **Effective capacitance** $C_{\text{eff}}$: Occurs at $V_{\text{op}}$ and is measured with an applied ripple voltage of 0.5 V AC (RMS) and 1 kHz. The CeraLink is designed to have its highest capacitance value at the operating voltage $V_{\text{op}}$.

- **Nominal capacitance** $C_{\text{nom}}$: Is the value derived by the tangent of the mean hysteresis (as the derivative of the mean hysteresis is $dQ/dV \sim C$).

See our [CeraLink Technical Guide](#) for further details.
Symbols and terms

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>$C_0$</td>
<td>Initial capacitance @ 0 V DC, 0.5 V AC (RMS), 1 kHz, +25 °C</td>
</tr>
<tr>
<td>$C_{\text{eff, typ}}$</td>
<td>Typical effective capacitance @ $V_{\text{op}}$, 0.5 V AC (RMS), 1 kHz, +25 °C</td>
</tr>
<tr>
<td>$C_{\text{nom, typ}}$</td>
<td>Typical nominal capacitance @ $V_{\text{op}}$, quasistatic, +25 °C. See glossary for definition of the nominal capacitance</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent serial inductance</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent serial resistance</td>
</tr>
<tr>
<td>$I_{\text{op}}$</td>
<td>Operating ripple current, root mean square value of sinusoidal AC current</td>
</tr>
<tr>
<td>LP</td>
<td>Low profile</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>PLZT</td>
<td>Lead lanthanum zirconium titanate</td>
</tr>
<tr>
<td>$R_{\text{ins}}$</td>
<td>Insulation resistance @ $V_{pk, \text{max}}$, measurement time $t = 7 \text{ s}$, +25 °C. For pre- and post-measurements within the scope of the AEC-Q200 reliability tests.</td>
</tr>
<tr>
<td>$R_{\text{ins, typ}}$</td>
<td>Insulation resistance @ $V_{\text{op}}$, measurement time $t \geq 240 \text{ s}$, +25 °C</td>
</tr>
<tr>
<td>SAC</td>
<td>Tin silver copper alloy; lead-free solder paste</td>
</tr>
<tr>
<td>$T_{\text{amb}}$</td>
<td>Ambient temperature</td>
</tr>
<tr>
<td>$\tan \delta$</td>
<td>Dissipation factor @ 0 V DC, 0.5 V AC (RMS), 1 kHz, +25 °C</td>
</tr>
<tr>
<td>$T_{\text{device}}$</td>
<td>Device temperature. $T_{\text{device}} = T_{\text{amb}} + \Delta T$ ($\Delta T$ defines the self-heating of the device due to applied current).</td>
</tr>
<tr>
<td>$T_{\text{max}}$</td>
<td>Max. device temperature, $T_{\text{max}} = +150 \text{°C}$. Reference temperature for reliability tests</td>
</tr>
<tr>
<td>$V_{\text{op}}$</td>
<td>Operating voltage at maximum attenuation capability</td>
</tr>
<tr>
<td>$V_R$</td>
<td>Rated voltage for $T_{\text{device}} \leq T_{\text{max}}$. Depends on the temperature derating defined on page 4 and can be higher than $V_{R, \text{max}}$</td>
</tr>
<tr>
<td>$V_{R, \text{max}}$</td>
<td>Rated voltage for $T_{\text{max}}$. Reference DC voltage for reliability tests</td>
</tr>
<tr>
<td>$V_{\text{AC (RMS)}}$</td>
<td>Root mean square value of sinusoidal AC voltage</td>
</tr>
<tr>
<td>$V_{pk, \text{max}}$</td>
<td>Maximum peak operating voltage (e.g. voltage overshoots or surge pulses which occur &lt;5% of total component lifecycle). Not for continuous operation.</td>
</tr>
<tr>
<td>$\Delta T$</td>
<td>Increase of temperature during operation</td>
</tr>
</tbody>
</table>
Cautions and warnings

General

- Not for use in resonant circuits, where a voltage of alternating polarity occurs.
- Not for AC applications. Consult our local representative for further details.
- If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.
- Do not use CeraLink components for purposes not identified in our specifications, application notes and data books.
- Ensure the suitability of a CeraLink in particular by testing it for reliability during design-in. Always evaluate a CeraLink component under worst-case conditions.
- Pay special attention to the reliability of CeraLink devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).
- Depending on the individual application, CeraLink components are electrically connected to voltages and currents, which are potentially dangerous for life and health of the operator. Installation and operation of CeraLink must be done only by authorized personnel. Ensure proper and safe connections, couplers, and drivers.
- Caution: CeraLink components are highly efficient charge storing devices. Even when disconnected from a supply, the electrical energy content of a loaded component can be high and is held for a long time. Always ensure a complete discharging of the component (e.g. via a 10 kΩ resistor) before handling. Do not discharge by simple short-circuiting, because of the risk of damaging the ceramic.
- Electrical charges can be generated on disconnected components by varying load or temperature. Caution: Discharge a CeraLink before connecting it to a measuring component/electronics, when this component is not sufficiently voltage proved.
  See Important notes section for further details.

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the lifetime of CeraLink devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases, the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.
Operation

- Use CeraLink only within the specified operating temperature range.
- Use CeraLink only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink can produce audible noise due to its piezoelectric characteristic.
- CeraLink components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of the manufacturer.

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The ordering code for one and the same product can be represented differently in data sheets, data books, other publications, on the company website, or in order-related documents such as shipping notes, order confirmations and product labels. The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products. Detailed information can be found on the Internet at www.tdk-electronics.tdk.com/orderingcodes.
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2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified**. In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.

3. **The warnings, cautions and product-specific notes must be observed.**

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