Passive embedding

Thanks to new materials and integration technologies, the embedding and integration of passive components is making great advances. New miniaturized components designed specifically for embedding enable even more compact and reliable systems.

The dimensions of passive components and their ruggedness for further processing often determine whether they are suitable for specific embedding and integration technologies. TDK has developed innovative capacitors and thermistors and employs state-of-the-art integration technologies that enable superior passive embedding solutions.

Embedding capacitors in IGBT modules

Traditionally, IGBT modules in the mid power range and based on Si and SiC technologies employ external snubber capacitors. Until now, it was not possible to embed these components and thus shorten the long leads that are afflicted with parasitic inductances. Irrespective of their dimensions, conventional capacitors are insufficiently resistant to the heat involved in the direct assembly of the IGBT module. In addition, some have only a low capacitance per volume and suffer considerable loss of capacitance at high rated voltages.

Now, with the TDK CeraLink™, a completely new kind of capacitor has been developed that suffers none of these drawbacks. CeraLink technology is based on the ceramic material PLZT (lead lanthanum zirconate titanate). In contrast to conventional ceramic capacitors, CeraLink has its maximum capacitance at the application voltage, and this even increases proportionately to the share of the ripple voltage (Figure 1).

![Figure 1: Capacitance of the TDK CeraLink as a function of voltage. In contrast to other capacitor technologies, the effective capacitance of the TDK CeraLink rises with increasing voltage. The impact of the ripple voltage amplifies this effect additionally.](https://www.tdk-electronics.tdk.com)
Another advantage is its high insulation resistance. The RC time constant \( \tau \) is 70000 \( \Omega \)F at 25 °C and this value drops only slightly even at 150 °C. As a result, this prevents the feared uncontrolled thermal runaway from occurring. Its parasitic effects are also very low: ESR is only 50 m\( \Omega \) at 100 kHz and drops to only 10 m\( \Omega \) at 1 MHz, resulting in very low losses. The ESR declines even further as the temperature rises: At 85 °C it is already less than 20 percent of its original value at 25 °C. This results in charge and discharge times of between 25 ns and 30 ns. The ESL of CeraLink capacitors is below 5 nH, making this technology particularly suitable for fast-switching inverters.

All these advantages make CeraLink technology predestined to be embedded in IGBT modules as snubber capacitors. Two SMD types with rated voltages of 500 V DC are available for this purpose (Figure 2). The low-profile 1 \( \mu \)F variant with dimensions of only 4.35 mm \( \times \) 7.85 mm \( \times \) 10.84 mm and the 5 \( \mu \)F type with dimensions of 13.25 mm \( \times \) 14.26 mm \( \times \) 9.35 mm are particularly compact and may be placed very close to the semiconductor with negligible ESL.

![Figure 2](image-url)

**Figure 2:**
TDK SMD CeraLink for integration in IGBT modules:
The CeraLink low-profile 1 \( \mu \)F variant (left) and the 5 \( \mu \)F type (right) are designed for embedding in IGBT modules. They feature compact dimensions and can withstand high temperatures of up to 150 °C.
Embedding temperature protection in IGBT modules

IGBT modules in inverters achieve the highest possible efficiency when they are operated at their upper temperature limit. Thus, exact monitoring of the operating temperature is required in order to prevent damage to the semiconductors. The suitability of standard SMD NTC thermistors used for this purpose up until now, however, is rather limited because they are not compatible with all semiconductor assembly processes. In particular, these include high-temperature soldering and silver sintering under pressure.

The new components are now able to withstand the thermal and mechanical stresses encountered during assembly. Moreover, they save space because they need no special pads for soldering to the semiconductor substrate. In order to solve this problem, a wafer-based manufacturing process for EPCOS chip NTC thermistors was developed (Figure 3).

Figure 3:
Wafer and EPCOS NTC thermistor with contacts on the top and bottom surfaces:
Complete EPCOS NTC wafer with carrier (left) and an individual NTC chip (right). The flat contact areas are on the top and bottom surfaces, rather than on the sides, which is more usual.

A key advantage of the NTC thermistors manufactured from wafers is the configuration of their electrical contacts, which are located on the top and bottom surfaces of the chip. This allows the lower terminal to be contacted directly and with complete surface contact onto the semiconductor substrate using conventional semiconductor processes. The upper terminal is contacted via conventional wire bonding, as is usual for IGBT modules. The contact surfaces are optionally available in gold or silver plating in order to achieve the best possible bonding results.
Among the other advantages of these chip NTC thermistors are their minimal electrical and thermal tolerances. This precision is achieved by means of a special process technology: Before separating the individual elements from the wafer, the total resistance of the wafer is measured with respect to a rated temperature of 100 °C. The size of the thermistors to be separated is then determined based on this. This ensures that the tolerances of the separate components is much smaller than those of standard NTC thermistors rated at 25 °C (Figure 4).

![Figure 4: Comparing the precision of NTC technologies:](image)

Because EPCOS chip NTC thermistors have a narrow tolerance of only ±1.5 K at 100 °C, IGBT modules can then be operated without premature derating at temperatures very close to their maximum permissible values and thus be utilized more efficiently. This solution is also suitable for new power semiconductor generations such as those based on SiC and GaN.

### 3D integration with LTCC

As smartphones and other portable electronic devices are designed to support more bands and offer greater functionality, a maximum level of integration that goes beyond the miniaturization of the single components is required in order to keep these devices compact. LTCC technology (low temperature co-fired ceramic) is an established technology that enables the functions of passive components such as inductors, capacitors and resistors to be embedded within the thin ceramic layers. Depending on the level of integration, LTCC technology, which is used mainly to manufacture RF modules for smartphones, can save up to 80 percent space compared with discrete solutions.

However, because the LTCC sintering process takes place at temperatures higher than 500 °C, heat-sensitive components such as semiconductors must be mounted in piggyback mode on the upper side of the modules after sintering.
Semiconductor integration with SESUB

By actually embedding the ICs in the substrate, TDK’s SESUB technology (semiconductor embedded in substrate) represents a new approach to integration. Even including the embedded ICs, the overall thickness of the SESUB substrate is only 300 µm (Figure 5).

The discrete passive components required can be placed on the surface of the substrate. In order to increase the integration density even further, thin passive components will also be embedded in the substrate in a next step. Because SESUB modules make use of the third dimension, their area is 50 to 60 percent smaller than conventional discrete solutions, depending on the design.

The shorter line connections within the substrate layers of the modules lead to improved parasitics and thus support better system performance. EMC performance is also improved due to the shielding effect of the metal layers inside the SESUB substrate. In addition, SESUB delivers excellent thermal attributes due to the fact that the IC is completely embedded. All surfaces of the chip are in full contact with the laminate, which optimizes the heat transfer from the semiconductor into the substrate layers. These layers themselves contain the copper micro-interconnection grids, which provide for a very homogenous and efficient heat dissipation. In particular, their superior thermal performance is important for applications in the area of power management, transceivers, processors, and the power amplifier – or all the main components of a smartphone. In addition to miniaturization, key criteria for the use of both LTCC and SESUB technologies are their high reliability and significantly reduced logistics outlay.
A typical example of a SESUB design is the extremely compact TDK Bluetooth 4.0 low energy module, developed for the Bluetooth 4.0 low energy (LE) specification, which is being marketed as Bluetooth Smart (Figure 6 left). With a footprint of only 4.6 × 5.6 mm$^2$ and a low insertion height of 1 mm, the new SESUB-PAN-T2541 Bluetooth 4.0 LE module sets the industry benchmark for Bluetooth Smart modules. The module is also very well suited for use in wearable devices thanks to its compact size.

![Space-saving TDK SESUB module:](image)

**Figure 6:**
Space-saving TDK SESUB module:
Left: The TDK Bluetooth low energy module was developed for the Bluetooth 4.0 low-energy (LE) specification and is the world’s smallest with dimensions of only 4.6 mm x 5.6 mm. The complete power management of a smartphone is integrated in the TDK power management unit (right).

SESUB is also highly suitable for handling the power management in smartphones. In the TDK power management unit (PMU) module (Figure 6 right), the IC for managing the power supply was embedded directly into the substrate for the first time. This innovative step allows manufacturers of end equipment to reduce their development costs and times still further. In combination with newly developed capacitors and power inductors in SMD versions, the module dimensions are only 11.0 mm × 11.0 mm × 1.6 mm. They also contain a highly efficient power supply for the buck converter in a 5-channel configuration with an output current of up to 2.6 A as well as low-noise, high-PSRR (power supply rejection ratio), low-dropout regulators for up to 23 channels and an extremely efficient charge circuit for lithium-ion rechargeable batteries.

### Utilizing the integration potential of PC boards

Multilayer PC boards have long ceased to be merely carriers of components. In order to utilize their integration potentials more efficiently, TDK is working jointly with partners on the further development of technologies for embedding active and passive electronic components. Among other things, the standardization of the integration technologies, which play a critical role in the implementation of highly miniaturized modules, is to be driven forward.

Especially the MLCCs that are needed in nearly every circuit for buffering and noise suppression offer significant potential for integration and thus miniaturization. TDK has developed the MLCC-CU series, which can be embedded in PCBs. Unlike conventional MLCCs, their electrodes are not tin-plated, but rather made of copper and inserted directly into the laminate layers of the PC boards. These MLCCs are distinguished by their very low insertion heights of between 0.11 mm and 0.25 mm (Table).

<table>
<thead>
<tr>
<th>Table: TDK MLCC-CU-series for embedding in PCBs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shape: CUA1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>CUA1</th>
<th>CUA2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. capacitance [μF]</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>Length [mm]</td>
<td>0.6</td>
<td>1.0</td>
</tr>
<tr>
<td>Width [mm]</td>
<td>0.3</td>
<td>0.5</td>
</tr>
<tr>
<td>Max. insertion height [mm]</td>
<td>0.11 to 0.25</td>
<td>0.11 to 0.25</td>
</tr>
<tr>
<td>Terminal width [µm]</td>
<td>230</td>
<td>350</td>
</tr>
</tbody>
</table>