

**White Paper**

# xEVCap Next Level Capacitor Bank and thermo-mechanical evaluation of a powertrain inverter

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**Abstract**

Building on prior studies introducing the modular [xEVCap](#) DC-link solution and its system-level electro-thermal evaluation, this paper presents a validated thermo-mechanical model of a traction-inverter DC link using four xEVCap in parallel. The model, calibrated against a hardware demonstrator, predicts internal hot-spot temperatures and informs lifetime estimation. We assess a busbar design and fixation strategy (adhesives/gap fillers) that withstands automotive vibration while preserving low ESL and solderability. The modelling workflow powers the [CLARA](#) web tool's Capacitor Banks module, enabling rapid design-space exploration for 400/800-V inverters without prototyping.

**1. Introduction: xEVCap as DC-link capacitor solution**

xEVCap is the modular, scalable, and fully standardized DC-link capacitor solution offered by TDK for traction inverter systems with forced cooling [1, 2]:

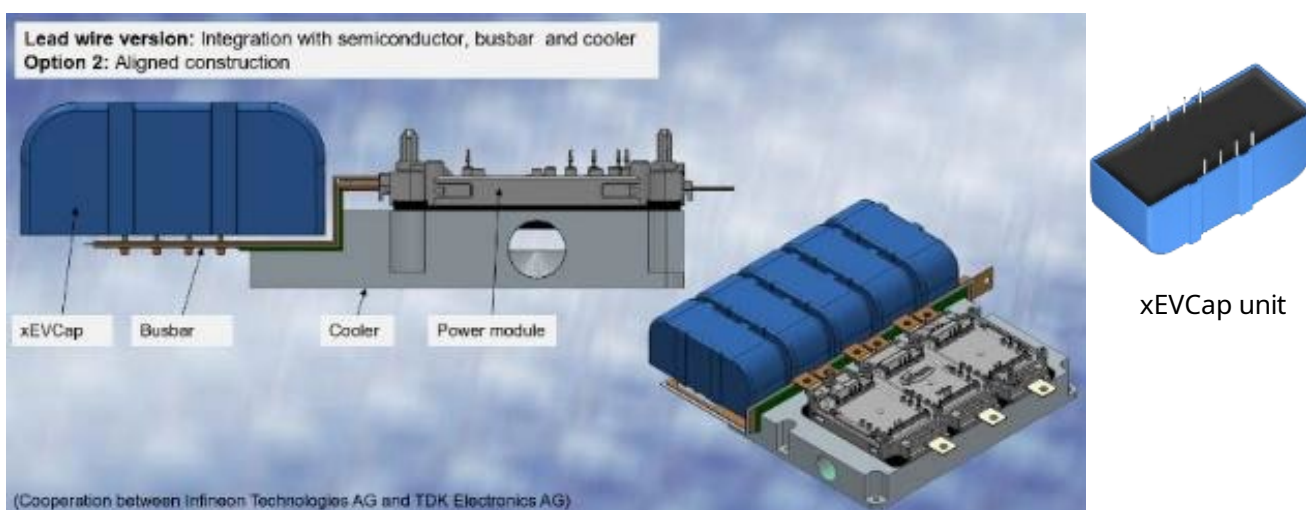


Figure 1. Example of use. It allows building any 400V / 800V traction system from 20kW and above by paralleling units.

$C_N$ (120 Hz) [ $\mu$ F]	Dimensions (L x W x H) [mm]	Ordering code	$I_{max}$ (10 kHz) [A]	ESL (1 MHz) [nH]	ESR (1 MHz) [m $\Omega$ ]	$\hat{I}$ [kA]	$I_s$ [kA]
<b><math>V_R = 500</math> V (DC); <math>V_{max} = 525</math> V; <math>V_s = 665</math> V</b>							
200	85 x 47 x 40.5	B25654A5207K*	40	17	1.13	2.1	6
270	109 x 47 x 40.5	B25654A5277K*	50	17	0.89	2.8	8
<b><math>V_R = 650</math> V (DC); <math>V_{max} = 750</math> V; <math>V_s = 900</math> V</b>							
115	97.5 x 35.5 x 42.5	B25654A6117K*	60	14	0.51	2	6
130	85 x 47 x 40.5	B25654A6137K*	42	17	0.89	1.6	5
175	109 x 47 x 40.5	B25654A6177K*	55	17	0.66	2.2	6.5
<b><math>V_R = 850</math> V (DC); <math>V_{max} = 890</math> V; <math>V_s = 1200</math> V</b>							
80	97.5 x 35.5 x 42.5	B25654A8806K*	56	14	0.57	1.7	5.2
100	85 x 47 x 40.5	B25654A8107K*	40	17	1.04	1.4	4.2
135	109 x 47 x 40.5	B25654A8137K*	50	17	0.78	1.9	5.8
<b><math>V_R = 920</math> V (DC); <math>V_{max} = 950</math> V; <math>V_s = 1250</math> V</b>							
60	97.5 x 35.5 x 42.5	B25654A9606K*	55	14	0.65	1.5	4.7
75	85 x 47 x 40.5	B25654A9756K*	35	17	1.18	1.2	3.8
110	109 x 47 x 40.5	B25654A9117K*	45	17	0.89	1.6	5.1

Table 1. Product range with given parameters like capacitance, footprints, ESL, ESR, and currents.

As observed in Figure 1 and Table 1, any user can design his own traction inverter without the need of a customized DC-link capacitor. It is only necessary to have an overlapped busbar or PCB for the assembly to the power semiconductor devices. The internal capacitor design offers inherently very low parasitics and good current ( $A_{RMS}$ ) balance when placed in parallel symmetrically to the power modules, as observed in Figure 2.

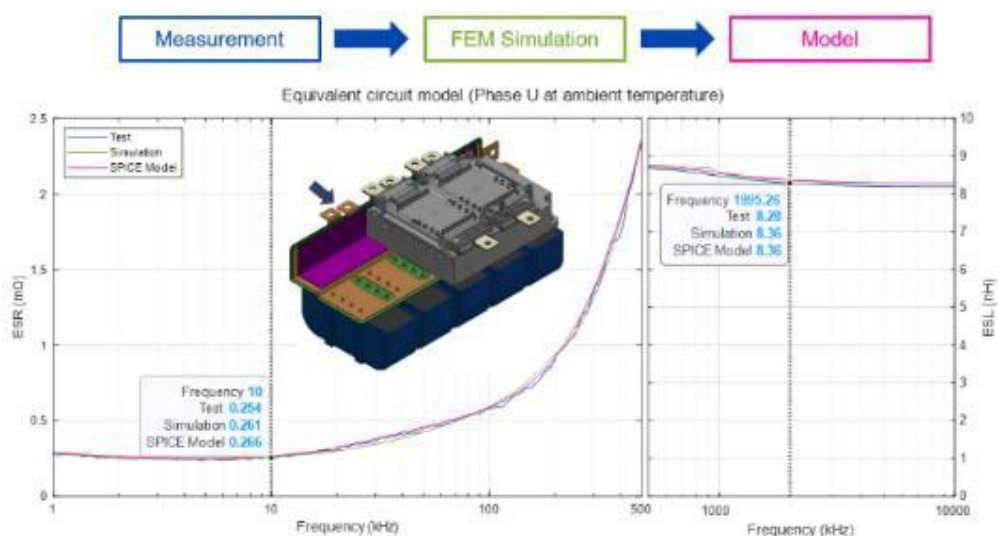


Figure 2. ESR (left) and ESL (right) vs frequency of a complete system with 5xB25654A8137K001- Test vs. Simulation vs. model.

The design of the busbar is key to easing the mounting of the capacitors by using conventional selective wave soldering, which was deeply developed under [2] by using soldering islands and tinned lead wire terminals for the capacitor elements. The integration with the cooler was also proposed under [2] to reduce the heat generated by the semiconductors reaching the capacitors (Fig. 3). That maximizes the current injected into the capacitor and therefore increases the power density of the system.

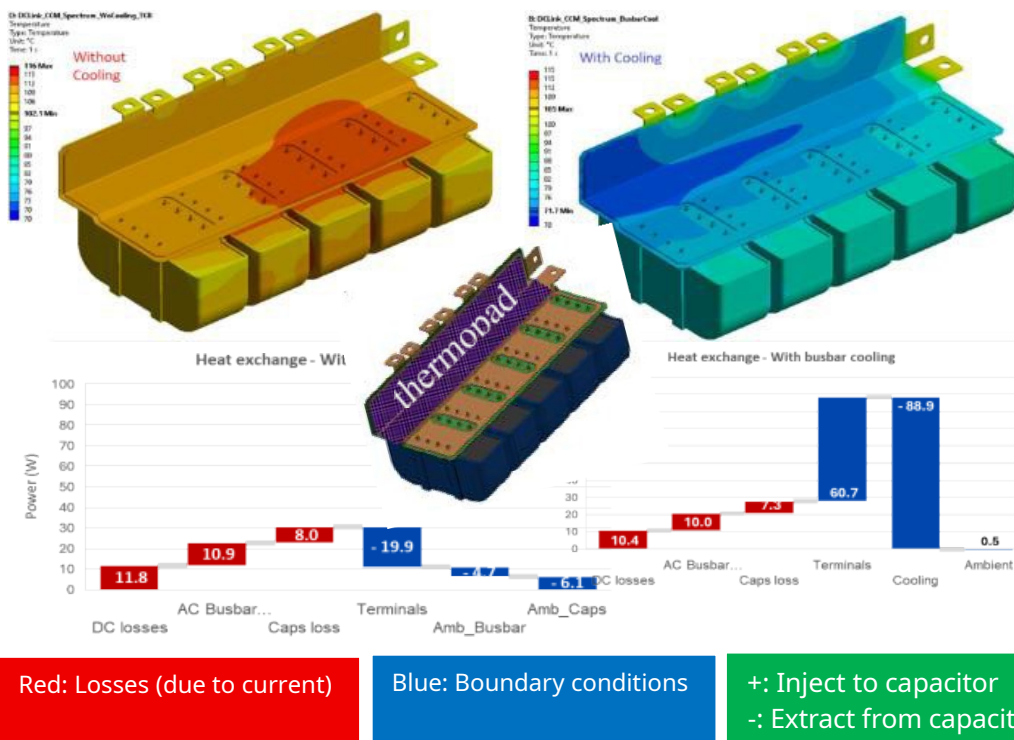


Figure 3. Proposed cooling strategy and proved benefits.

A demonstrator was built to prove the different cooling scenarios [2] under various load conditions (Fig. 4, Table 2).

## 2. Development of a simulation model of a whole system

The thermal characterization of this demonstrator was performed. A battery of different tests, as shown in Figure 4, was executed, and the key interactions between the components were deeply evaluated:

- **Interface with the cooler:** in the proposed system, the cooler is in direct contact with the DC-link busbar. The main objective of this cooling interface is to achieve a thermal decoupling between the semiconductor terminals, where the effect of their higher temperature is minimized in the capacitor. For that purpose, a combination of different water inlet temperatures and flow rates was considered.
- **Interface with the semiconductor (through busbar terminals):** the interaction with the semiconductor modules is critical for the DC-link capacitor operation. Power modules operating temperatures can reach values up to +175 °C, with thermal management being one of the main aspects of the converter design. Their higher operational temperatures translate into a higher temperature at the terminals of the DC-link capacitor, which has lower rated temperatures (+105 °C). For this demonstrator, the temperature of the terminals is controlled via a set of PID-controlled heaters, so different operation modes can be emulated.



Figure 4. Demonstrator with cooler, water flow and heaters to simulate different scenarios of cooling and different temperatures.

All tests are carried out under room ambient temperature and natural convection with the surrounding air. Power losses are introduced via a high-frequency power supply, injecting an RMS current of 168 A at 20 kHz (pure sinusoidal) in the complete system. With electromagnetic characterization of the module, loss generation from the current input is 19.1 W.

Test No.	$f_{I,AC}$ [kHz]	Water temperature [°C]	Busbar / semiconductor temperature [°C]	Water flow rate [L/min]	Active cooling
1a	20	without cooler	not controlled	N/A	N
1b		50	70	8	Y
2a	20	60	80	8	Y
2b			80		Y
2c			90		Y
2d			100		Y
2e	60	80	5	Y	

Table 2. Testing different cooling scenarios under various load conditions

The temperatures were monitored on the main positions, to assess the effect of each boundary condition on the complete system and the thermal characterization results (empirical tests) were discussed in [2]. For new capacitor DC-link solutions, results obtained with thermal characterization tests provide vital information for thermal modelling. All measured data is used to tune simulation models. The main advantage of thermal simulations at system level is the possibility to obtain internal temperature maps, with information from otherwise unreachable points, i.e. the internal temperatures of the capacitive elements (coils).

Among the tests of Fig. 4, the most critical case is **2d** (see Table 2). The temperature at the terminals where the semiconductor would be connected, it is fixed at 100°C, and the water temperature is set at 60°C. Fig. 5 shows a comparative graph between the simulation and the test results, and the differences between them (in red dotted line, right axis).

Figure 6 shows the thermal results of the complete system and a section of the central capacitor (A-A). For the testing case **2d**, the capacitor hotspot is +85.9 °C, located at the central xEVCap element. Thermal model accuracy is validated by comparison with the measured data from thermocouples in the empirical test.

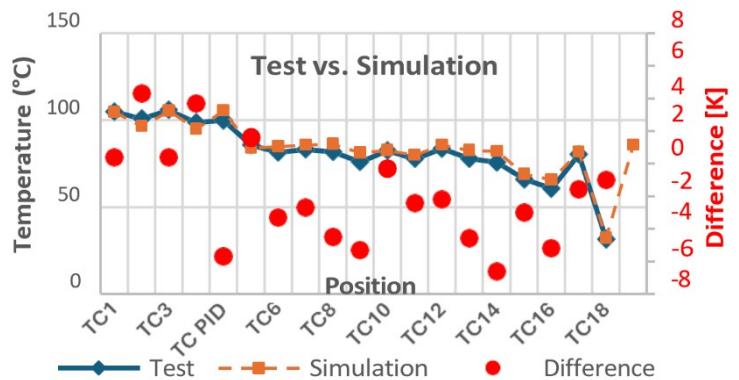


Figure 5. Thermal simulation results for test number 2d

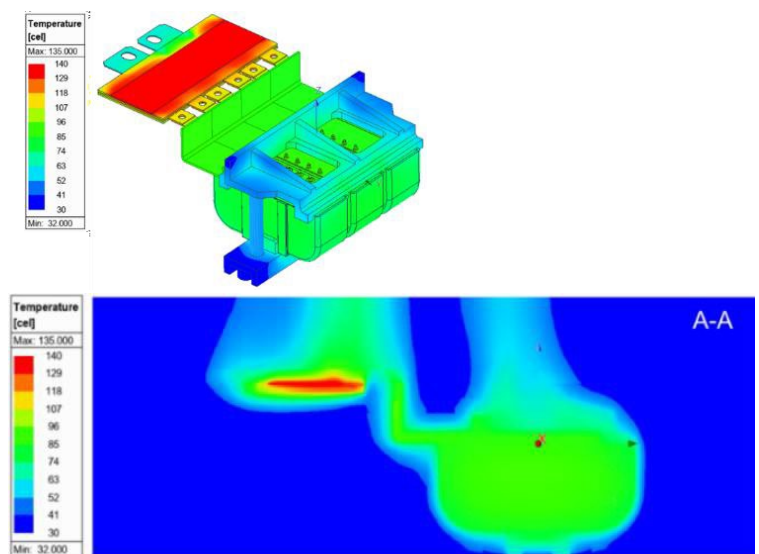


Figure 6. Isometric view of the thermal simulation results for case 2d. (Bottom) Section A-A of thermal simulation as an example of access to internal temperatures.

- All monitored points compared to the simulation show differences within  $\pm 7$  K. This inaccuracy is due to:
- Cooling influence simplification: The combination of natural convection with the air and the complexity of the cooler internal geometry and water flow was limited due to the available computing power. Considering that one of the objectives of these tests is to evaluate the influence of the different capacitors placed with low separation between them, the interface with the cooler was simplified. The temperature at the interface surface between the cooler and the thermopad is defined based on the measured temperatures at the cooling blocks.
  - Influence of supporting structures: All supporting structures for the test create heat conduction interfaces with the test environment. For the test, it

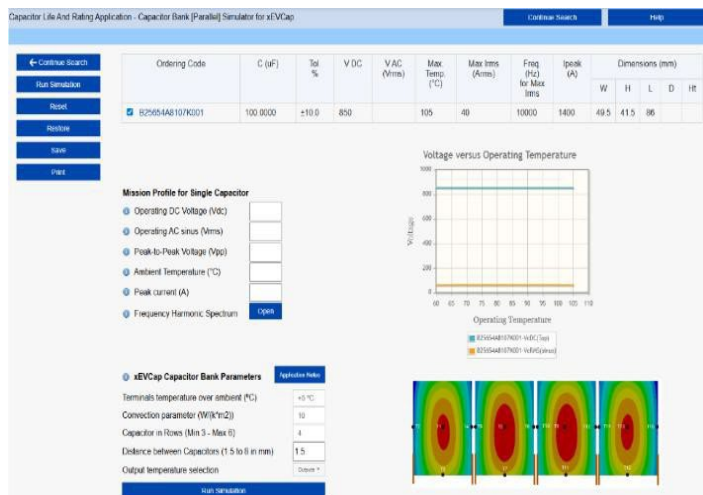


Figure 7. Capacitor Banks module for xEVCap (Web application CLARA – Capacitor Life and Rating App)

## 2.1. xEVCap Capacitor Banks web application

With the modelled system, validated with empirical tests, the virtual characterization methodology is validated for the evaluation of a whole system under different application conditions, and therefore the modelling tools. One of these tools is the xEVCap Capacitor Banks web simulation tool integrated in TDK's [CLARA web application \(Capacitor Life and Rating App\)](#). This tool allows system designers to obtain instant thermal behavior insights for xEVCap capacitor systems under a variety of application conditions. The obtained thermal results are then used as inputs for expected lifetime estimations and safety margins of the selected capacitor solutions under the given conditions.

Figure 7 shows an image of the input required to run the module. Designers can simulate between three and six xEVCap capacitors in parallel, working as a DC-link solution.

The required inputs to run the thermal model are the minimum set of application values that are needed to perform a quick estimation of the system behavior: ambient temperature, frequency harmonic spectrum, terminals temperature over ambient, convection parameter, and distance between capacitors.

Additional input parameters, such as operating DC and AC voltages, peak current, etc., are then used for the lifetime and safety margin estimations. A similar tool is also implemented for PCB mounted capacitor matrix. In that case, thermal evaluation is done considering forced air cooling conditions. Both online tools have been validated with thermal tests of representative cases with natural cooling conditions (for xEVCap modules) and a forced cooling testing system (for PCB-mounted arrays).

## 3. Mechanical evaluation of a complete system

xEVCap does not have external screw fixations like traditional customized capacitor block solutions, which need a customized integration into

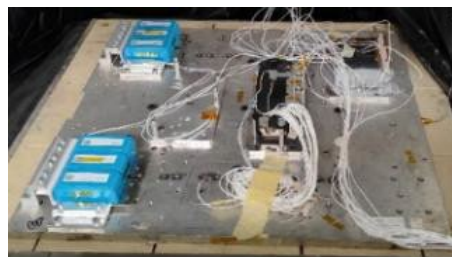


Figure 8. Setup (left) and fracture of the solder islands (right). The capacitors were not glued or fixed to the busbar.

the traction inverter system. xEVCap is a modular unit whose lead-wire terminals are designed for high current, not for structural retention. Vibration test performed (resonance search from 5 Hz to 2000 Hz at -40 °C, room temperature, and +105 °C, and random test according to IEC TS 63337 and ZVEI standard) exposed the weakest element of the whole assembly: the solder islands at the capacitor to busbar interface,

which fractured (Fig. 8) under vibration when the unit was free mounted, without use of fixations or adhesives. That was done on purpose to detect the weakest link from a mechanical point of view.

This observation sets the design target: provide a holistic fixation concept, including adhesives, gap filler, and stack clamping, that preserves the proven solderability and electrical performance demonstrated in the previous work [2], while withstanding automotive thermo-mechanical stress. Such an approach is widely adopted for PCB-mounted capacitors in automotive systems.

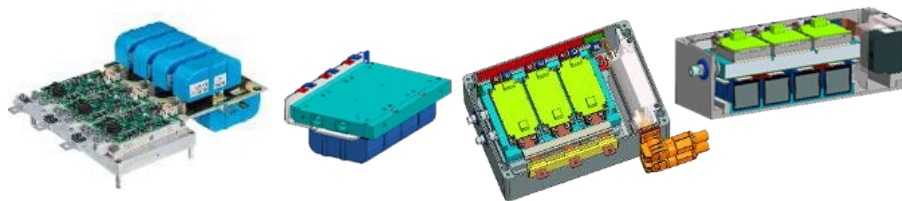


Figure 9. Infineon EconoDual™ (left) and views (from left to right) of the system proposed: xEVCap with cooler, Busbar and xEVCap B25654A8137K001, Full system with open lids, System cross-section.

For that purpose, a new system inverter is proposed. The new demonstrator derives from Infineon's EconoDUAL™ 3 power kit. It retains the cooler, gate driver and power module layout, and replaces the DC-Link capacitor bank of eight xEVCap (75 μF/850 V) by four xEVCaps in parallel (B25654A8137K001, 135uF-850V,

lead wire version), which is a common reference design for around 250-300kW power systems [1][2]. And altogether with a new busbar, connectors, and EMC filter (TDK [CarXield](#), B84252B0400A000).

The busbar design builds upon the sandwich construction approach introduced in a prior study [2], but with a specific focus on optimizing the soldering process for capacitors while improving the vibration robustness. To achieve this, a localized “island” geometry is incorporated around the lead wire terminal, which concentrates thermal energy at the soldering point (Fig 10).

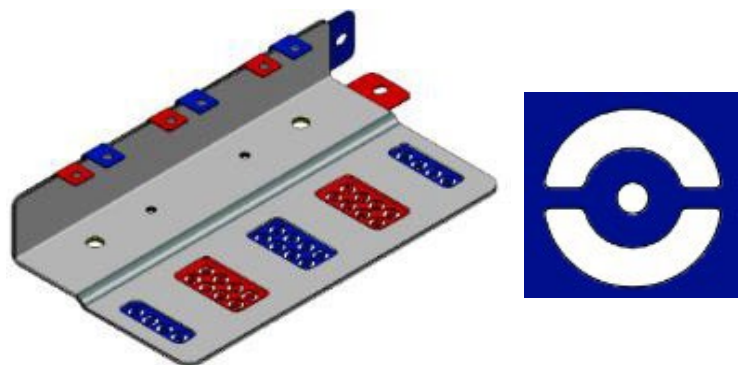


Figure 10. Busbar design and soldering island

Regarding the average busbar costs, these vary depending on the manufacturing method and the order quantity. Figure 11 illustrates the evolution of unit price based on quantity and method. For small batches (fewer than 3,500 units), laser cutting is the most cost-effective option. For larger quantities, single stamping becomes the cheapest method overall. Continuous stamping is only worthwhile for very high-volume production (above 15,000 units).

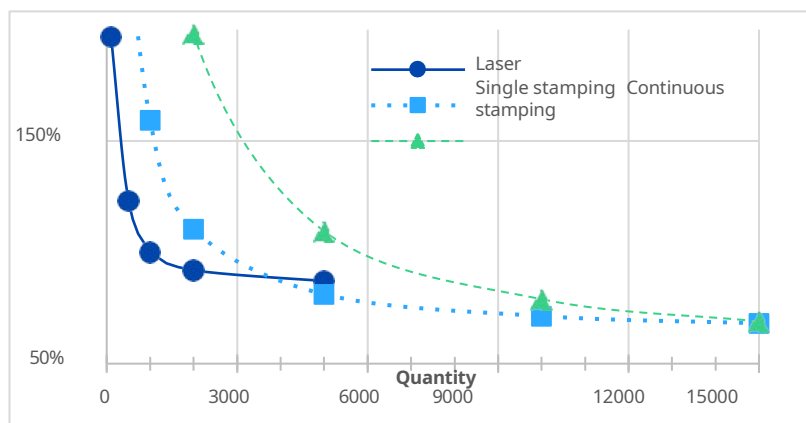


Figure 11. Unit price (including mold) vs Quantity. Prices are normalized for 1k units by the laser method

Mechanically, the cooler is bolted to the housing, and the busbar is clamped to the cooler. Two screws close the stack (power module plus busbar with capacitors), and four screws fix this stack to the housing. For all the screws used in the system, dry torque targets are M4 = 3 Nm, M5 = 6 Nm, M6 = 10 Nm, M8 = 25 Nm, with A2-70 bolts into aluminum AW5083. Internal trials confirmed an M6 failure around 26 Nm, providing a comfortable safety margin.

To damp resonances and open a parallel heat path, the capacitors are bonded to the

busbar using room temperature vulcanizing (RTV) silicones. Additionally, gaps between capacitor cases and housing are filled using liquid thermal interface materials. Two suppliers were selected (Shin-Etsu and a supplier called "B" for this paper). For adhesives, KE4901W (from Shin-Etsu) and B-9 (from supplier B) were compared, showing similar adhesive behavior.



Figure 12. (Left) Manual mixing with supplier Shin-Etsu with gap filler KE1897S A/B. (Center) Supplier B with gap filler B-5 manual mixed. (Right) Recommended pneumatic gun for a proper mix.

For gap fillers, B-5 (Supplier B, 2.0 W/(m·K) paste) is compared with KE1897S A/B (Shin-Etsu, 2.1 W/(m·K) potting). B-5 showed challenges for filling: high viscosity in nature, observed as per technical specifications,

voiding, and incomplete cure with the manual mixing as per our basic laboratory methodology used. Supplier B recommended the use of a pneumatic dual-component cartridge gun that would avoid this improper mixing and unstable result (Fig. 12).

KE1897S A/B delivered reproducible curing with 3 hours at +100 °C with similar manual mixing (meeting the +105 °C capacitor hot spot limit). Due to the better appearance, KE1897S A/B was selected for the complete demonstrator (Fig. 13), while supplier B products were applied in a dummy for mechanical testing. Both systems are considered mechanically equivalent and tested under the same conditions.

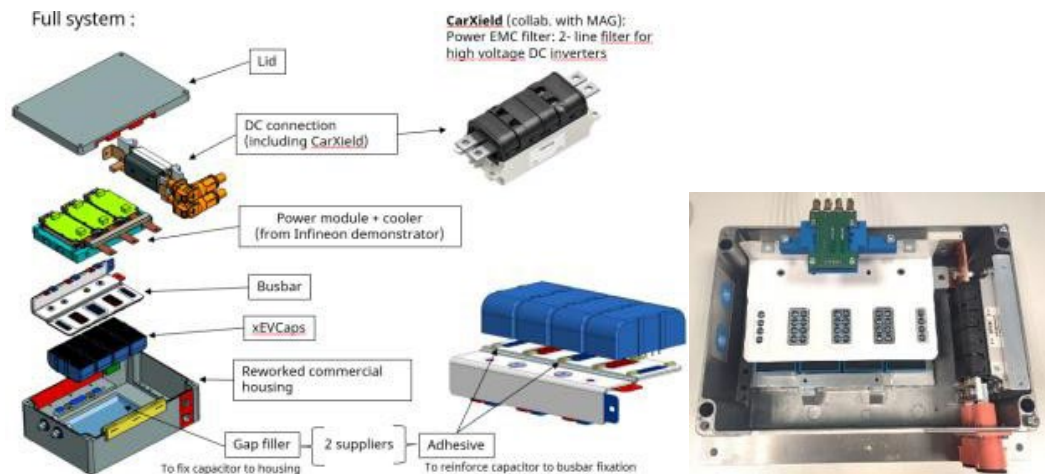


Figure 13. Detail view of the proposed powertrain inverter demonstrator. (Right) Demonstrator with measuring jig for Electrical characterization.

### 3.1. Electrical characterization: Busbar design for ESL optimization

The assembled DC-link capacitor was electrically characterized using a custom fixture to ensure accurate impedance measurements at the same points where semiconductor modules would normally connect. The results confirmed stable capacitance and ESR values across the frequency range. No

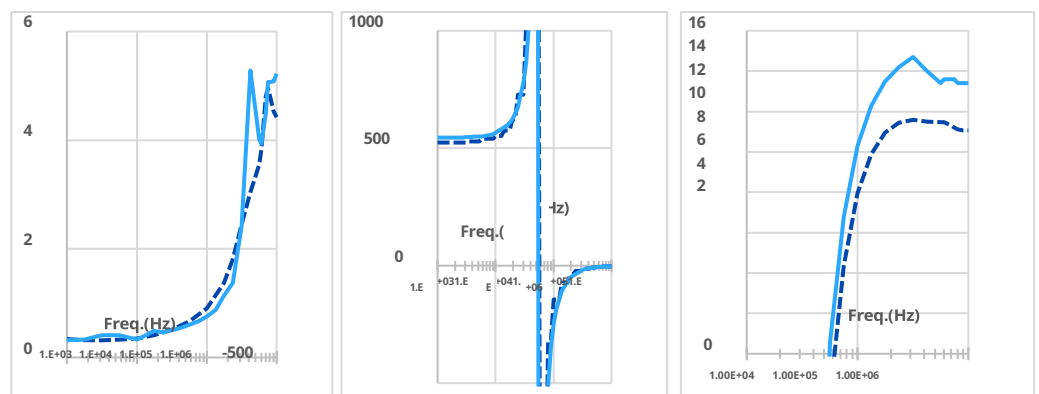


Figure 14. Simulation (dark blue-dashed) vs real measurement (light blue).

anomalies were detected in the soldered lead-wire joints, which maintained low parasitic inductance and resistance within the expected design envelope. As a double check, an electromagnetic simulation was carried out to virtually characterize the system, comparing ESR and capacitance values against the measured data (Fig. 14).

Minor differences between simulated and measured values were observed, which can be attributed to the measurement fixture used during testing, introducing slight parasitic measurement effects not modelled in the virtual environment.

Previous systems with another busbar design [2] (supplier A), had resulted in lower total parasitic loop inductance, in the range of 8nH. While for this demonstrator, the value is at the level of about 11nH (supplier B). This led to an analysis of both busbar constructions, measuring the overlapped area and making different simulations with slight changes in the geometry to evaluate how it affects the inductance. The key findings were:

- The localized “Soldering Island” geometry around the lead wire terminal does not significantly affect the inductance of the whole system.
- The overlapped area is much higher in supplier A busbar (8 nH), and it reduces the inductance directly. Especially in the busbar terminals connected to the power module.

However, for the present demonstrator, increasing the overlapped area is quite complex because:

- The sandwich construction does not allow for reducing the distance between the terminals connected to the power module (Fig. 15).
- Increasing the overlapped area implies the reduction of the creepage distance, and Supplier B is not in favor of doing that. The insulation sheet could not be correctly bonded, risking the electrical insulation.
- The busbar (11 nH, Supplier B) has been designed more simply, prioritizing the cost with less use of material per unit of power.

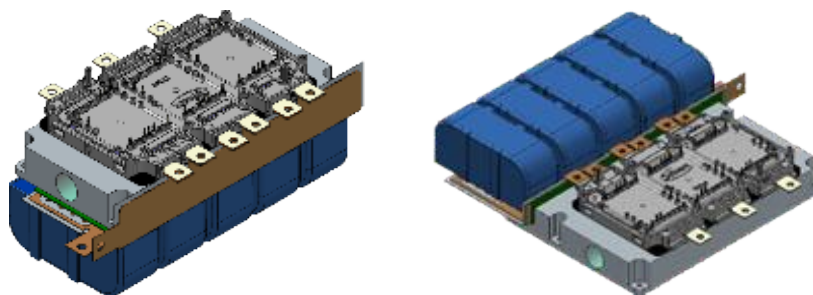


Figure 15. (Left) Example of a sandwich construction. (Right) Example of an aligned construction with a shorter length between the capacitors and semiconductors.

Future designs must balance these factors to achieve both low inductance and cost-effectiveness in traction systems. The inductance of non-overlapping conductor segments followed an equation dependent on geometry, with the total length of non-overlapping conductors being the dominant factor in ESL increase.

$$L_{flat} = 2 \cdot 10^{-4} \cdot \left[ \ln \left( \frac{2 \cdot l}{w + t} \right) + 0.5 + 0.2235 \cdot \frac{w + t}{l} \right]$$

With  $L_{flat}$ : inductance of the conductor [ $\mu$ H];  $l$ : length of the conductor [mm];  
 $w$ : width of the conductor [mm];  $t$ : thickness of the conductor [mm] [4,5,6]

Applying this equation, the terminals connected to the power module contribute +2.6 nH to the total inductance in this new demonstrator, which is roughly the difference between the two busbar designs.

### 3.2. Thermal evaluation

To comprehensively assess the reliability of the demonstrator system, a thermal simulation was conducted under typical operating conditions (Fig. 16). This evaluation aimed to verify the system’s ability to dissipate heat effectively and maintain component temperatures within safe operating limits. Thermal simulations predicted a maximum hotspot temperature of +99 °C on the film capacitor, remaining comfortably below the +105 °C maximum value specified in the xEVCap datasheet.

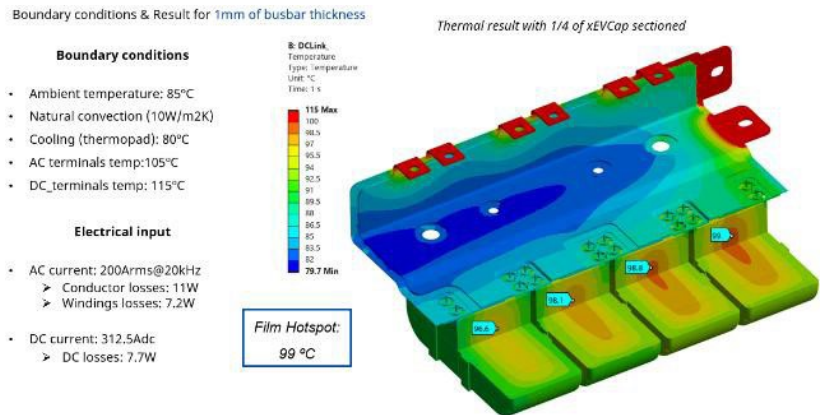


Figure 16. Thermal simulation with operation parameter

Further validation was performed through thermal stability test, conducted both before and after vibration testing, which aims to check the absence of abnormal heating or localized hotspots under 200 A (RMS) and 10 kHz, replicating high-load automotive conditions. Thermocouples and infrared thermography (Fig. 17) are employed to detect potential hotspots at solder joints and capacitor bodies, which were not found.

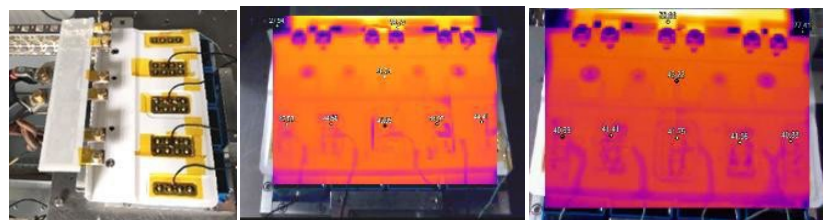


Figure 17. Thermal stability test (200 A, 10 kHz) before and after vibration test, not showing remarkable differences.

### 3.3. Vibration test

The vibration test aims to detect potential weaknesses in the components themselves at the mechanical level, but also at the system level. The component-level standards (AEC-Q200, IEC TS 63337, or CarXield datasheet) provide vibration parameters, type of stress (random or sinus), but do not define how the component must be fixed into the whole system. And in fact, vibration requirements at the whole system level may differ from the ones at the component level, as observed in the following table. Results, positive or negative, will depend on how the capacitor is fixed in the system.

	Acceleration (RMS) [m/s <sup>2</sup> ]	Frequency band [Hz]	Test duration (per axis) [h]	Test duration (total) [h]	Temperature [°C]
xEVCap (AEC-Q200)	49 (sine)	10 ... 2,000	4 (20 min x 12 cycles)	12	room temperature
IEC TS 63337	30.8 (random)	2 ... 2,000	8	24	room temperature
CarXield	100 (random)	10 ... 2,000	22	66	-40 ... +85
CarXield	30; 60; 30 (sine)	100; 200; 440	22	66	-40 ... +85
System (example)	20 ... 60 (sine)	5 ... 2,000	till 40		-40 ... +85, and room temperature
System (example)	25 ... 50 (random)	2 ... 2,000	till 90		room temperature

Table 3. Vibration tests for different parts of the inverter system

For a reliable approach with full understanding of the use of xEVCap in real applications, xEVCap shall also be evaluated in a real system, using fixations and adhesives commonly used by the industry as in the demonstrator of Figure 13.

A sinusoidal vibration test according to the AEC-Q200 (as referred in the xEVCap datasheet) was conducted with positive results, demonstrating robust and reliable performance for both configurations: demonstrator with Shin-Etsu adhesive and gap filler, and a dummy with the materials from Supplier B (Fig. 18).

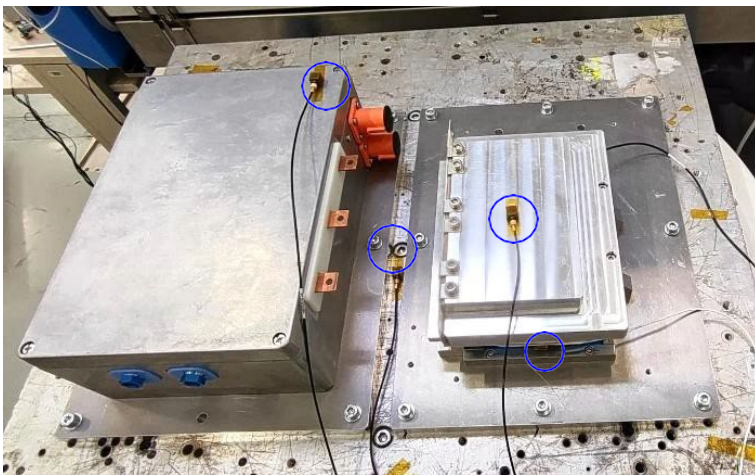


Figure 18. Demonstrator assembly and vibration testing setup (accelerometers locations marked). (Left) Full Demonstrator with Shin-Etsu.

To ensure a comprehensive validation of the design, the demonstrator underwent visual inspections, electric characterization, and thermal stability assessments both before and after the vibration test. This comparative approach enabled a precise identification of any potential degradation or material fatigue resulting from mechanical stress. As illustrated in Figure 19, a detailed view of the busbar soldering following the vibration test confirms that no physical damage, such as cracking, deformation, or loosening of connections, occurred. Furthermore, the consistency between the pre-vibration and post-vibration thermal data further validates that the internal electrical paths and interfaces remain secure and unaffected.



Figure 19. Detailed view of the soldering island after vibration tests

Additionally, the demonstrator was subjected to high-voltage step testing at 850 V and 1000 V, with each voltage held for a duration of 60 seconds at room temperature. The system

withstood these elevated electrical loads with no signs of dielectric breakdown or insulation failure. These findings indicate that the proposed fixation and damping approach is highly effective and suitable for the xEVCap demonstrator.

#### 4. Conclusion and Future Work

The knowledge about the usability of the TDK xEVCap as a standard modular DC-Link Capacitor solution for traction inverters has been extended to the next level. While in previous papers [1,2], the product, the system, and its electromagnetic and thermal aspects were covered, now there is a complete thermal model of a system.

This model is helping our customers to simulate under different scenarios of current load and temperatures, in just a few computing days, without building prototypes. Web tools, like the Capacitor Banks in CLARA (TDK, Capacitor Life and Rating Application), help the customer to select, simulate, design, and even order samples of the desired capacitor module.

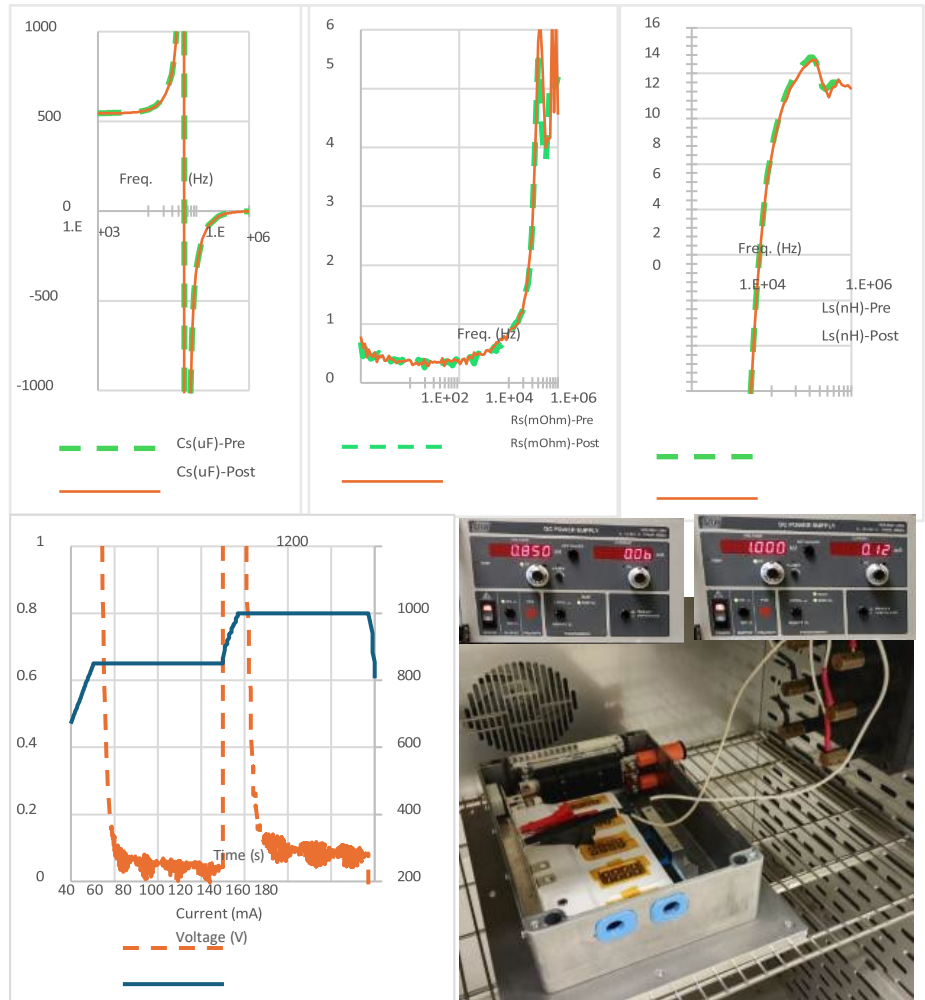


Figure 20. Electrical parameters (before and after vibration) and high-voltage test with leakage current measurement at 850 V and 1000 V. No abnormalities were detected.

The results of the vibration test of the demonstrator have provided a validated approach and critical insights for the mechanical integration of the xEVCap in the Traction Inverter, including the type of adhesives and gap fillers, and design aspects of the busbar. These results will be used to feed our simulation systems, elevate our models to establish dependencies with temperature, and therefore provide advanced support for our customers to design and optimize their traction inverter systems.

## ACKNOWLEDGMENT

To all contributors not explicitly mentioned, but providing technical information and useful learning lessons. Special thanks for their valuable contributions to Infineon Technologies AG and Shin-Etsu Silicones Europe B. V

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