White Paper

Introduction to xEVCap
A modular DC-link capacitor solution for the main powertrain inverter of xEVs

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Abstract
This paper describes a novel approach for a DC-link film capacitor for the main power train of xEVs. With an understanding of the challenges and requirements, the approach targets standardizing the capacitor design for this application. A design concept of the capacitor is validated with simulations and laboratory test data. The paper does not intend to disclose all aspects of product design and process, but it will show why it can be a flexible solution for system engineers through its modularity and usage. These capacitors are connected through an external busbar to the power modules (and these to the motor) and additional circuitry, such as the battery or EMI filters. This standardized approach will simplify the development efforts for circuit designers as well as engineering costs.

Introduction: The DC-link capacitor in the main traction inverter of an electric vehicle

The DC-link capacitor acts as an energy buffer between the input and output in the power converter. Its core mission is to keep the DC voltage stable, which means within the defined voltage limits by the system (also called the smoothing function). While being charged from the input, this capacitor supplies the necessary current to the power semiconductors (and these to the output load with the target voltage-current waveform). This general concept of DC-link capacitors applies to any power converter system and, thus, any end application, from small power adaptors to wind power converters in the megawatt range.

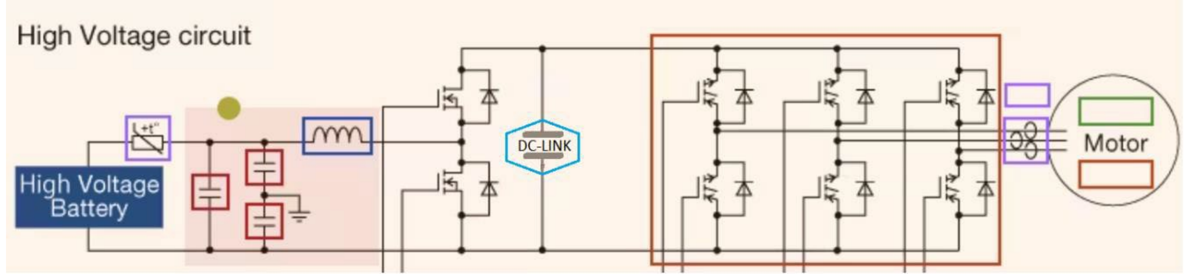

Figure 1. Block diagram example of a motor inverter including an EMI filter, DC-DC converter, and main traction inverter. The DC-link capacitor is highlighted with a blue hexagon.

Multiple capacitor technologies can be used as a DC link, and their suitability depends on voltage, power range, application, etc. [1]. Even several capacitor technologies can be used in the same system, one to cope

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with lower-frequency current harmonics and another with higher frequency harmonics, responding to the nature and demand of every system design in connection with the properties of every capacitor technology.

For example, the snubber capacitor, which is parallel to the DC-link capacitor, is placed very close to the power semiconductor, targeting a minimum parasitic inductance. This snubber capacitor manages the highest frequency current, reducing voltage overshooting by providing the necessary current when required. So, it aims to compensate for the higher parasitic inductance of the main DC-link capacitor bank. Thus, it is not always needed, as shown in Figure 2. The DC-Link bank of film capacitors supplies the high-frequency harmonics of current with minimum parasitic inductance, so the film capacitors assume the DC-link and snubber roles, the same as the DC-link capacitor in the main traction inverter of xEVs.

Figure 2. Demonstrator of a 1500 V solar inverter by Infineon. Easy 3B module: 1200V TRENCHSTOP™ IGBT7 + 1200 V CoolSiC™ MOSFET. TDK Electronics: Hybrid DC-link capacitor bank: High-frequency film capacitor (blue) + aluminum electrolytic (black) [2].

Capacitance, voltage, current capability, and temperature range are the initial key parameters to identify which capacitor technologies are suitable as a DC link for each system requirement. When multiple technologies are available, system designers must also consider the pros and cons of every technology because they must cope with the non-ideal characteristics of these components:

– Parasitic inductance (ESL) and resistance (ESR),
– Thermal behavior and limits
– Reliability
– Complex behaviors with frequency, voltage, temperature, aging, etc., when applicable
– Mounting
– Moreover, size and cost impact the whole system.

As a result, biaxially oriented polypropylene (BOPP) film capacitors are, as of today, the dominant technology solution used for the DC-link of the main traction inverter in xEV systems [3].

Among other well-established technologies for DC-link, polypropylene film capacitors offer (for this application and target power range) the necessary voltage ranges, energy, current density, lifetime, temperature handling, and reliability. In addition, they are solving well the challenges of introducing wide bandgap (WBG) semiconductors, proving that they can handle the increasing frequencies, A per µF, dV/dt, and ESL reduction strategies.

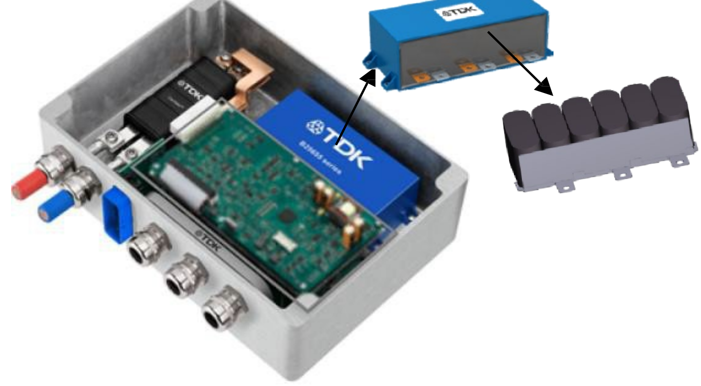


Figure 3. Reference design by Mankel-Engineering in collaboration with TDK and Infineon Technologies. 240 V (DC) to 475 V (DC) with a peak power of 120 kW at 400 V (DC). The capacitor rating is 650 µF/500 V [4], with an overview of internal construction made

The problem: Customizing the DC-link capacitor

The DC-Link capacitor is one of the bulkiest and most customized components in these xEV systems. The terminals are typically divided into three pairs, each for every half-bridge phase, as shown in Figure 1. The terminals (position, shape, size) must be adapted to every power semiconductor supplier and model to

minimize the stray inductance. As for DC-input terminals (not shown in the figure), their relative position and size depend on the overall system design, i.e., the power and position of the battery mains. The internal busbar design, winding element number, and arrangement must be adapted to the system requirements (capacitance, voltage, I_{RMS}, stray inductance, cooling, space, geometry, etc.).

The cooling system influences the internal design of the capacitor because it will influence the mission profile expected for the capacitor: voltage-capacitor temperature—% of lifetime. Vice versa, the internal capacitor design will determine the actual hot spot temperature for every I_{RMS} condition and, therefore, also the cooling system. This applies to everything with continuous changes coming from other subsystems or operational conditions during the design of a new vehicle, because the main traction inverter is only a part of it.

The consequence is iterative and long design cycles until system requirements are merged with the final capacitor design. A demand for higher capacitance to manage, for example, higher I_{RMS}, will result in the modification of the whole capacitor with its internal and external construction. Every seemingly minor change in the capacitor design significantly impacts engineering cost and time to market.

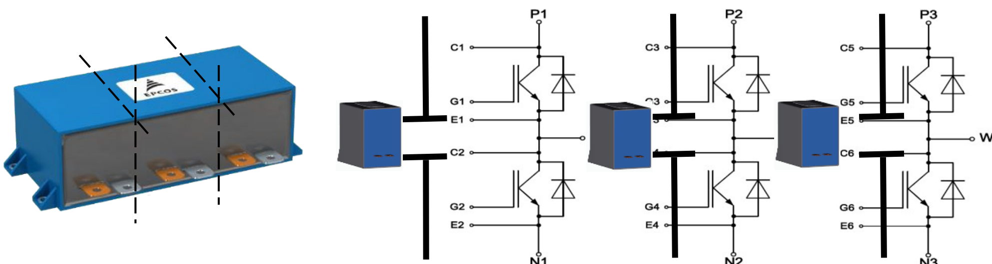


Figure 4. The basic concept is to divide the bulk customized capacitor into standardizable units.

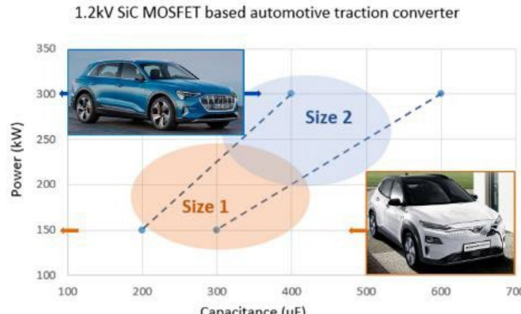


Figure 5. Basic system requirements.

For example, Plastic injection tooling for encapsulation, cutting-punching-bending tooling for busbars, related production processes, and all the production equipment for future automation—all these changes must be supported with the required validation testing and evaluation to maintain the required performance, quality, and reliability in a mass production scenario, not only at the component level but at the whole system level.

The Infineon evaluation kit "EVAL KIT HPD G1 SiC" [5] refers to a TDK capacitor with 300 µF/855 V (B25655P8307K351). That solution would need external busbar adaptation to add DC terminals.

The proposal: Design for application of a modular capacitor solution

This bulk customized capacitor solution is divided into standardizable capacitor units, as shown in Figure 4.

No capacitor unit can provide the full capacitance and power required by the traction inverter. Still, paralleling them through a laminated busbar with a compensated inductance arrangement makes it possible. This solution can be easily scaled to any power level, power semiconductor supplier, model, system geometry, or cooling. DC terminals and other accessories, like EMI filters, can be incorporated into the busbar.

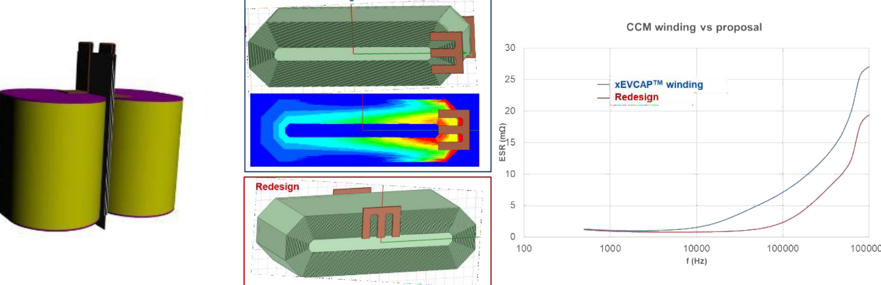


Figure 6. Left: Initial Internal structure with 2 winding elements in parallel and overlapped busbar. Center: Redesign proposals and thermal study. Right: ESR behavior depends on the terminal position.

Critical challenges were observed while designing this application's modular DC-link film capacitor. Firstly, mitigating parasitic inductance requires internal overlapping of busbars, which adds cost to the raw materials and production process. Secondly, based on the application frequency, there is a high chance of a non-homogeneous distribution of RMS currents inside the winding elements, as shown in Figure 5. That can limit current per capacitance for systems employing wide-bandgap semiconductors.

	Size 1		Size 2	
Power level	**Low**	**Mid**	**Mid-high**	**High**
C [µF]	200 – 300	300 – 400	375 – 525	400 – 600
$I_{c\,RMS}$ (max.) [A]	116	155	200	235
I_{dc} (max.) [A]	175	235	295	350
V_R [V]	850	850	850	850
P [kW]	150	200	250	300
$I_{ph.RMS}$ (max.) [A]	200	265	335	400

Table 1. Design to application (split by Power) of the modular DC-link capacitor approach

A redesign of the initial concept of Figure 5 (left) is based on a detailed review of present and future inverter power modules in the automotive domain, the cooling methodologies, and their electrical requirements, as shown in Figure 6: Rated power: 150 kW—300 kW; capacitance range: 200 µF to 600 µF. The target spectrum is divided into Size 1 for low and mid power and Size 2 for mid and high power.

Table 1 shows the extracted parameters of the DC-link capacitor linked to application parameters that will lead to the optimized design for the application: the ripple current flowing through the capacitors (Ic), the input current from the battery (I_{dc}), the rated voltage of the capacitor (V_R), the power of the system, and the output phase current (I_{ph}; modulation index 0.6 – 0.7). The DC-link capacitor is divided into individual units, paralleled, and connected through a busbar to the power semiconductors, as shown in Figure 7. All this is done with the support of simulation tools to verify its feasibility for the target specifications, such as the ESL, which is measured at the contact points of the semiconductor with the busbar.

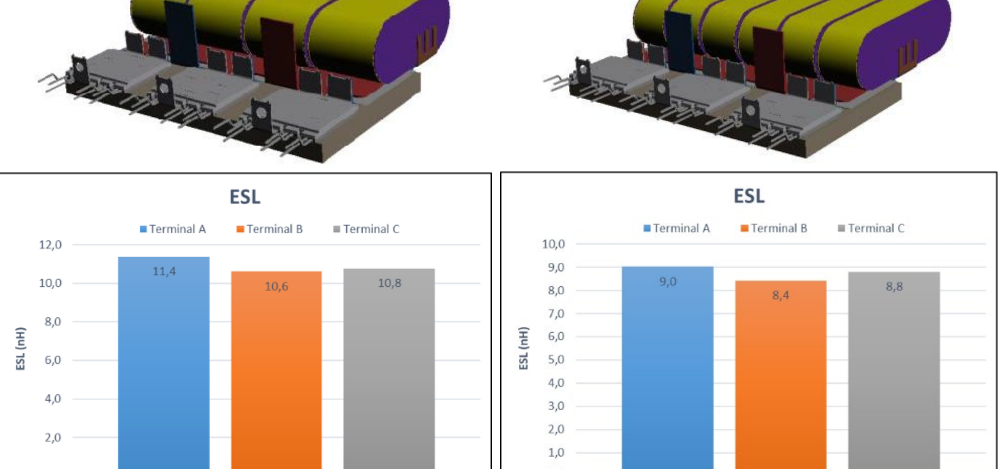
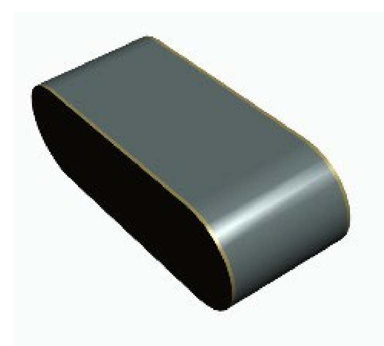


Figure 7. Modular concept design for DC-link applications; standardized solution compatible with power semiconductor modules. Left: Size 1 (400 µF); right: Size 2 (500 µF)

The product: xEVCap, design-for-manufacturing

Afterward, a design for manufacturing is developed, targeting standardization in terminal pitches and box sizes, like what is available for PCB components. The solution must be flexible and scalable for the target applications. Thus, a limited number of encapsulation box sizes and internal elements are proposed, maximizing capacitance and current handling for every module.



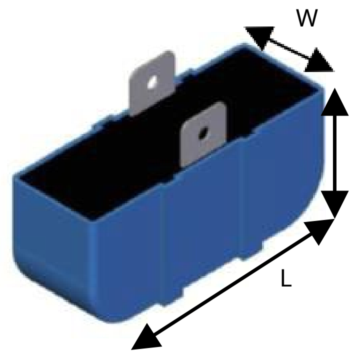


Figure 8. Encapsulation box (left), internal winding element (center), final xEVCap (right) for the DC-Link modular approach

C_R [µF]	$V_{R,DC}$ [V]	$I_{C,RMS}$ (max.) @ 10 kHz [A]	L_s @ 1 MHz [nH]	ESR @ 10 kHz [mΩ]	Dimension L x W x H [mm]
200	475	40	17	1.13	85 x 46.5 x 40.5
270	475	50	17	0.89	109 x 46.5 x 40.5
115	650	60	14	0.51	97.5 x 35 x 42.5
130	650	42	17	0.89	85 x 46.5 x 40.5
175	650	55	17	0.66	109 x 46.5 x 40.5
325	650	53	24	1.16	111.5 x 77 x 41.5
75	850	56	14	0.57	97.5 x 35 x 42.5
97	850	40	17	1.04	85 x 46.5 x 40.5
130	850	50	17	0.78	109 x 46.5 x 40.5
242	850	42	24	1.35	111.5 x 77 x 41.5
60	920	55	14	0.65	97.5 x 35 x 42.5
75	920	35	17	1.18	85 x 46.5 x 40.5
100	920	45	17	0.89	109 x 46.5 x 40.5
185	920	40	24	1.54	111.5 x 77 x 41.5

Table 2: xEVCap proposed range.

Table 2 provides the spectrum range and critical electrical and mechanical specifications of xEVCap. Four voltage levels, targeting 400-V (650-V-rated semiconductors) and 800-V systems (1200-V-rated semiconductors), are defined as such that, for example, a 920 V rating in the 800-V system provides a longer service life for demanding mission profiles, especially when temperature and voltage are high.

A narrower width (W) will increase the I_{RMS} per capacitance, while a longer length or height (L or H) will increase the energy density.

A system designer must consider the system's electrical and mechanical requirements and choose an appropriate capacitor module to match these requirements. Paralleling these units and connecting them through laminated busbars reduces the system ESR and self-inductance (ESL). This solution offers flexibility and scalability to system engineers because capacitance, I_{RMS}, ESL, and power could be adapted and scaled by placing multiple capacitor units in parallel.

The validation testing is done according to the following standards: ZVEI "Basic Qualification of DC-Link Capacitors for Automotive Use" [6] and AEC-Q200 [7] table for film capacitors. Some test results are illustrated in Figure 9.

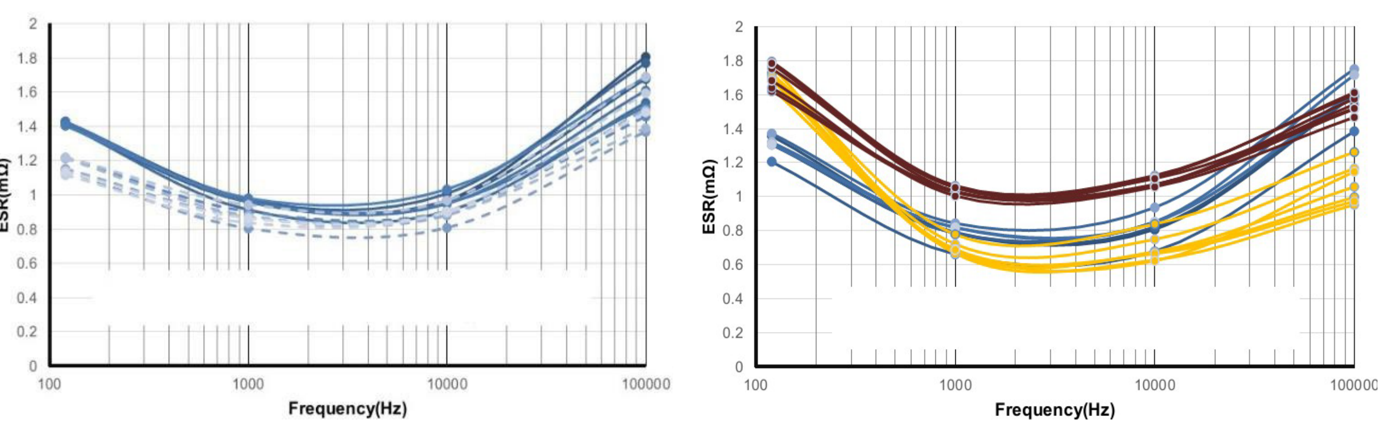


Figure 9(a). ESR vs. frequency; laboratory measurement of a device with 270 µF at 500 V (blue), with 115 µF at 700 V (yellow), with 130 µF (brown) and 175 µF both at 700 V (blue)

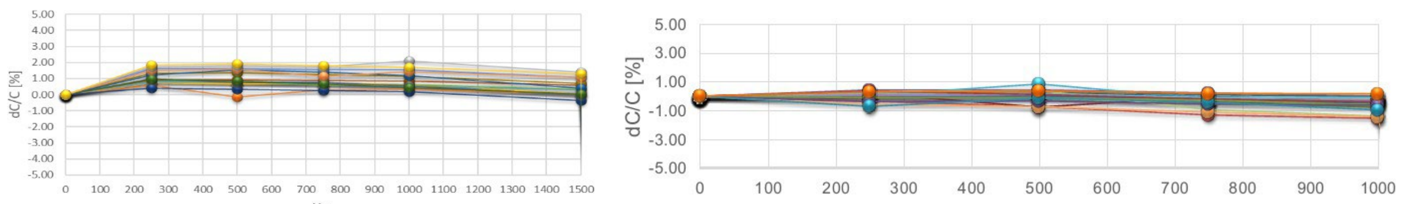


Figure 9(b). High-temperature operating lifetime according to AEC-Q200 [7], +105 °C, 1000 hours; 115 µF and 175 µF at 700 V (left), 75 µF at 850 V (right).

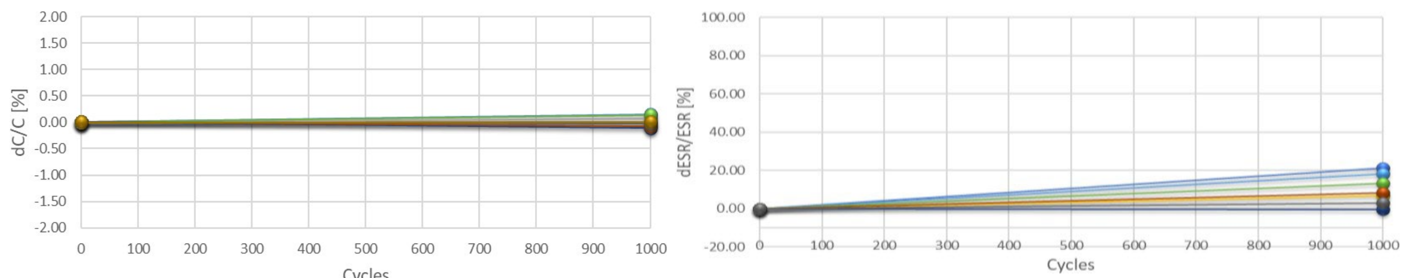


Figure 9(c). Thermal shock test according to ZVEI [6] from -40 °C to +105 °C for different sizes of 850 V rating.

Figure 9(d). xEVCaps during testing: High-temperature operating lifetime (left). Test fixtures for AEC-Q200 vibration test (center and right)

A real case: System design with xEVCap

The analysis of the inverter system requirements (like in Table 1) is the necessary starting point to scope the feasible modular approach for the DC-link capacitor solution with the xEVCap range shown previously in Table 2.

System requirement	Value
C (µF)	≥ 450
$I_{c\ RMS}$ (max.) [A]	250 ... 300
I_{dc} (max.) [A]	250 ... 300
V_R [V]	800 (900 for a limited time)
P [kW]	250
$I_{ph\ RMS}$ (max.) [A]	400 ... 500 (max. 650 for 10 seconds)
ESL [nH]	~7

Table 3: Analysis of system requirements (collaboration with STMicroelectronics)

Knowing how much electrical stress is really applied is important for voltage rating selection. Will a voltage level of 900 V, for example, occur continuously or in very short time periods? Will higher temperatures occur for long or short periods, or when the voltages applied to the capacitor are higher?

It is then beneficial to have an estimation of the mission profile over established operation cycles and lifetime, for example, driving (8000 h), preconditioning (5000 h), and charging (40,000 h). That will optimize the internal capacitor design through an adequate voltage rating defined by the dielectric thickness required to manage the expected voltages and temperatures applied during the whole lifetime. Higher safety margins will lead to larger and more costly solutions, while insufficient safety margins will require a redesign. These issues can be mitigated by using a standardized modular approach.

To fulfill the requirements in Table 3, two proposals from Table 2 with an 850-V rating are studied, one using six components of 75 µF each, expected to comply well with the electrical requirements; the other, with four components of 130 µF each, has fewer parts, more for cost-size efficiency, but with less performance. These are summarized in Table 4.

C_R [µF]	$V_{R,DC}$ [V]	$I_{C,RMS}$ (max.) @ 10 kHz [A]	L_s @ 1 MHz [nH]	ESR @ 10 kHz [mΩ]	Dimension L x W x H [mm]	Number of units (C_{total}, I_{RMS})
75	850	56	14	0.57	97.5 x 35 x 42.5	x6 (450 µF, 336 A) **Lower inductance, higher $I_{c\ RMS}$**
130	850	50	17	0.78	109 x 46.5 x 40.5	x4 (520 µF, 200 A) **Smaller size**

Table 4: xEVCap with two proposed options

Simulation tools are then used to analyze the feasibility of matching the system requirements and calculate the values for ESR and ESL. In the real application, the current in the capacitor (Ic) shall be decomposed into frequency harmonics (see Fig. 10). An evaluation considering only the fundamental switching frequency would underestimate the power losses because the ESR tends to be higher at higher frequencies. As a result, the thermal behavior and current balancing may be underestimated.

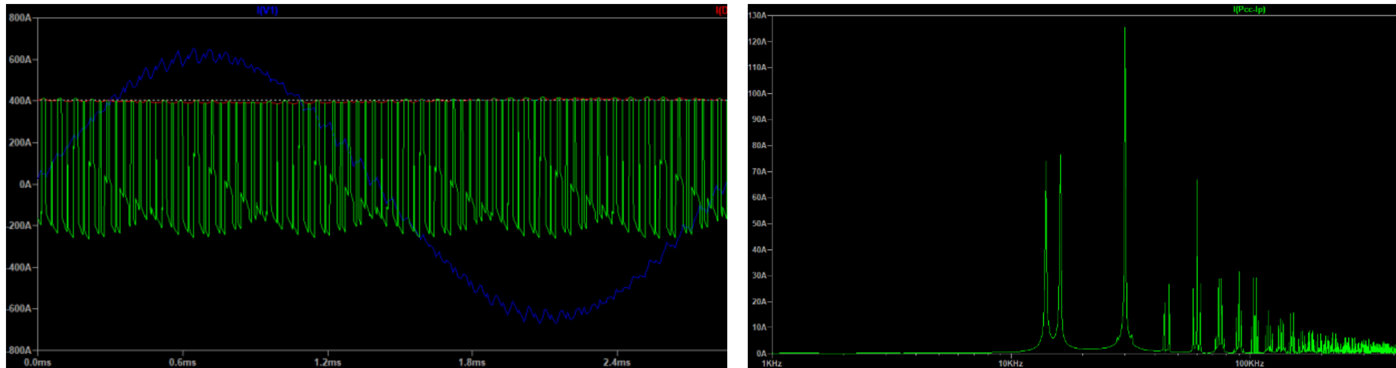


Figure 10: (Left) Simulation of inverter waveforms with I_{ph} (blue), I_{dc} (red), and capacitor current I_c (green). (Right) The frequency spectrum of I_c.

The simulation results (Fig. 11) show very low ESR values (note: scale is different), but the most important characteristic is almost perfect balancing from any of the three pairs of terminals corresponding to every phase. This indicates a balanced current for the studied frequency spectrum. Unbalancing would lead to uncontrolled hot spots in some areas of the capacitors that would limit their lifetime.

Figure 10. Top and center: ESR (top) ESL (center) vs. frequency curves for (left) 6 x 75 µF at 850 V vs. (right) 4 x 130 µF at 850 V.

The evaluation is done with SiC power semiconductors, proving that the xEVCap is fully compatible with wide-bandgap semiconductors in terms of inductance and current density. The DC-link solution with 4 x 130 µF offers 200 kW maximum power, while the one with 6 x 75 µF reaches up to 300 kW. This demonstrates its scalability and easy adaptation to a wide variety of systems, even those evolving during system design.

Figure 11. Double Side Cooling Power Module High Power traction inverter, and xEVCap mounted on the laminated busbar. The double-pulse test confirmed the simulated values of 8 nH for the DC-link capacitor solution (Collaboration with STMicroelectronics)

Conclusion and future work

A modular standard capacitor provides a flexible solution that reduces development time and simplifies design efforts while meeting the present performance requirements of DC-link capacitors for inverter power modules in xEVs – also for WBG semiconductors. Modularity ensures lower ESR, homogenous thermal distribution, and flexible adoption of cooling methodologies for the system designer. A future scope includes the use of higher temperature dielectrics with automatic temperature upgrades and higher energy densities, as well as a deeper study of the assembly techniques of capacitors to busbars, power semiconductors, and other circuitry like EMI filters.

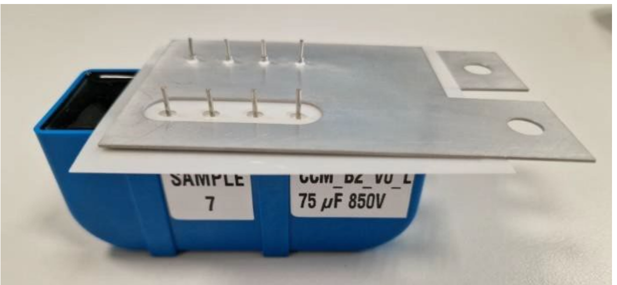


Figure 12. Future work-study: Study of joint technologies and terminations.

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