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White Paper

A Practical Use of xEVCap
The modular and standard DC-link capacitor solution for the main EV powertrain inverter

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Abstract

An innovative DC-link capacitor solution [1] for the main xEV powertrain Inverter has been presented to the market as of July 2024. The innovation is sustained by the conjunction of four pillars: modularity and scalability; design for application; design for manufacturing; and standardization (catalog product). After a brief review of these pillars already detailed in [1], this paper focuses on the practical study of xEVCap at the system level. The analysis is deployed in four major subject areas. The parasitics (ESL, ESR, ...) from the single capacitor element to the effective ones at the system level. The second area is the assembly and joint technologies with the busbar. The third area is the strategy for thermal decoupling between the capacitor and power semiconductors without a cooler. The paper concludes with the thermal integration with a cooler and how the various elements interact under different temperatures. Everything is supported by Ansys and CFD simulations, and with the construction of a demonstrator for laboratory testing. This paper also presents the results of collaboration with recognized external partners, such as power semiconductor and busbar suppliers.

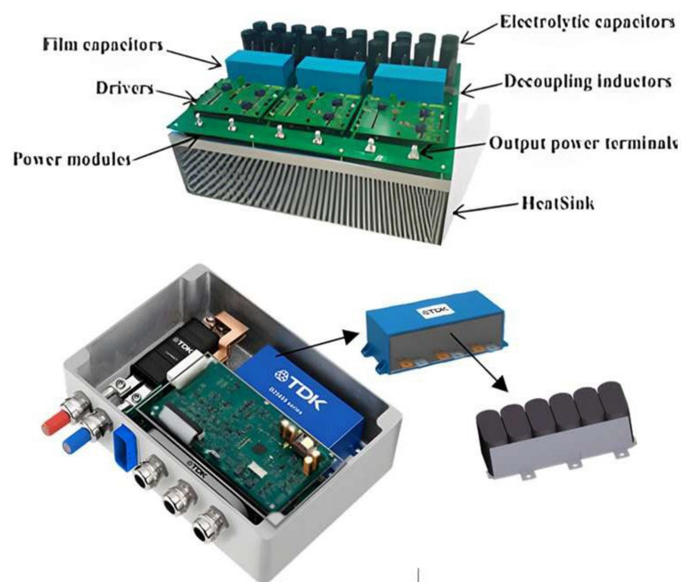

Figure 1. (up) Demonstrator of a 1500 V solar inverter by Infineon Technologies AG with Easy 3B module.
TDK Electronics: Hybrid DC-link capacitor bank: High-frequency film capacitor (blue) and aluminum electrolytic capacitors (black) [3].
(bottom) Reference design by Mankel-Engineering in collaboration with TDK and Infineon Technologies AG. Capacitor construction made with 6 parallel flat winding elements of polypropylene film capacitors.

xEVCap as DC-link capacitor solution

The DC-link capacitor acts as an energy buffer between the input and output in the power converter. Its core mission is to keep the DC voltage stable, which means within the defined voltage limits by the system (also called smoothing function). Multiple capacitor technologies can be used as DC-link (Fig. 1-Up), and their suitability depends on voltage, power range, application, etc. [2]. Biaxially oriented polypropylene

(BOPP) film capacitors are, as of today, the dominant technology solution used for the DC-link of the main traction inverter in xEV systems [4].

The DC-Link capacitor is one of the bulkiest and most customized components in xEV systems. If higher capacitance is required, for example, to handle a higher I_{RMS}, the entire capacitor with its internal and external design must be modified. The Infineon evaluation kit "EVAL KIT HPD G1 SiC" [6] refers to a TDK capacitor with 300 µF/855 V (B25655P8307K351). That solution would need external busbar adaptation to add DC terminals.

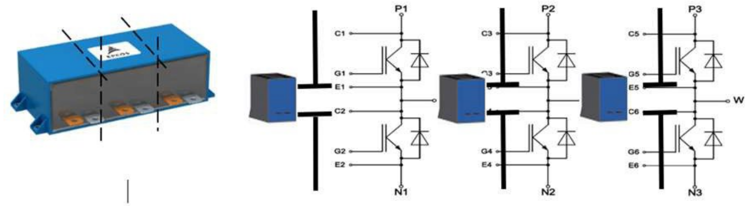

Figure 2. The basic concept was to divide the bulk customized capacitor into standardizable units.

The first pillar: Modularity and scalability

The bulk customized capacitor solution was divided into standardizable and modular capacitor units, as shown in Figure 2.

Each capacitor unit cannot provide the full capacitance and power required by the traction inverter. Still, paralleling them through a laminated busbar with a compensated inductance arrangement makes it possible. This solution can be easily scaled to any power level, power semiconductor supplier, model, system geometry, or cooling. DC terminals and other accessories can be incorporated into the busbar.

	Size 1		Size 2	
Power level	Low	Mid	Mid-high	High
C [µF]	200 – 300	300 – 400	375 – 525	400 – 600
$I_{C,RMS}$ (max.) [A]	116	155	200	235
I_{DC} (max.) [A]	175	235	295	350
V_R [V]	850	850	850	850
P [kW]	150	200	250	300
$I_{ph,RMS}$ (max.) [A]	200	265	335	400

Table 1 Design to application (split by power) of the modular DC-link capacitor.

The second pillar: Design-for-application

The target application spectrum was divided into Size 1 for low and mid-power and Size 2 for mid-high and high-power traction inverter systems. Table 1 shows the extracted parameters of the DC-link capacitor linked to typical application parameters.

The whole DC-link capacitor was divided into individual units, paralleled, and connected through a busbar to the power semiconductors, as shown in Figure 3, to offer the required capacitance and power.

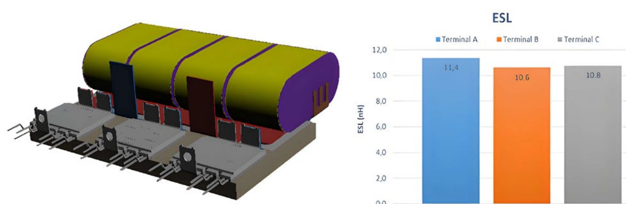

Fig. 3. Modular concept design for DC-link applications; standardized solution compatible with power semiconductor modules. Size 1 (400 µF).

A design for manufacturing was developed, targeting standardization in terminal pitches and box sizes, similar to what is available for PCB components. A narrower width (W) will increase the I_{RMS} per capacitance, while a longer length or height (L or H) will increase the energy density. Raw materials, design, and production tooling are optimized to allow scaled and automated mass manufacturing.

The third pillar:
Design-for-manufacturing

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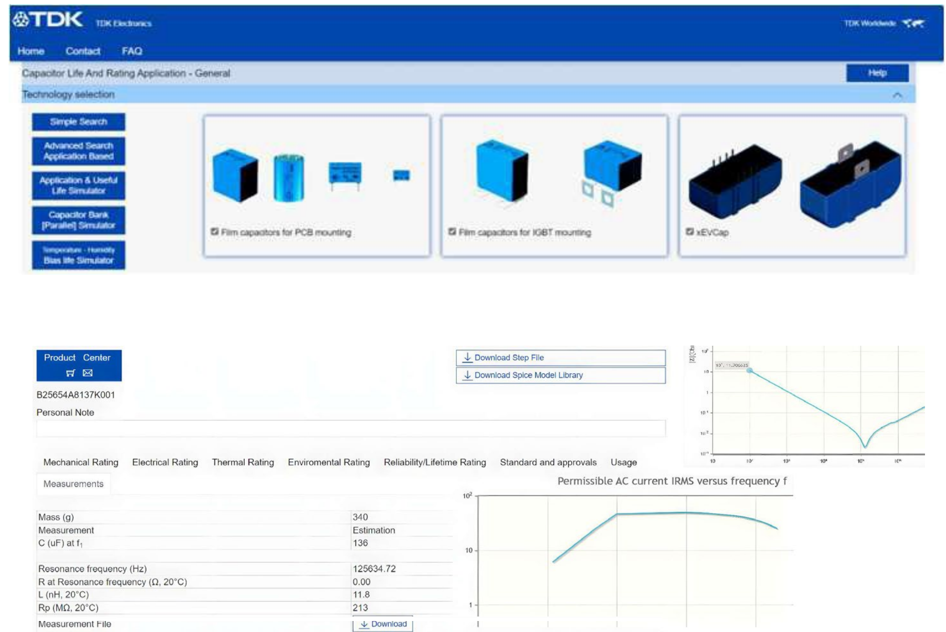


Figure 4. xEVCap product details fully available in the TDK-Electronics web for all designers under design-support/design-tools/film-capacitors/CLARA

Two types of terminals, four voltage levels, and three different footprints are fully available and included in the web search and simulation tool CLARA (Capacitor Life And Rating Application). This tool simulates the components electrically and thermally under different operating conditions, also providing detailed data like mechanical and electrical parameters, curves, 3D files, and complex SPICE models valid in the time and frequency domain.

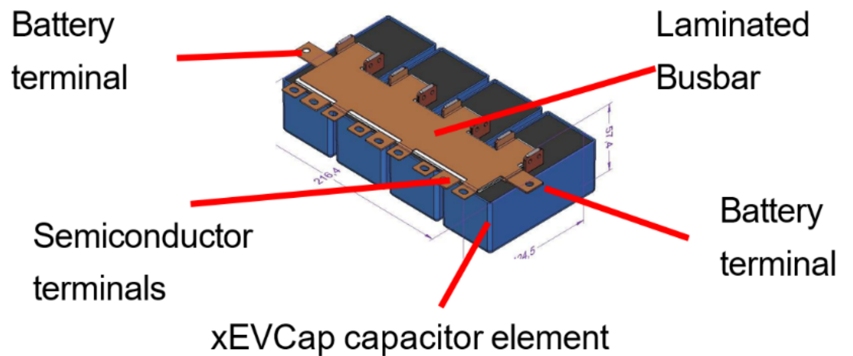


Figure 5. "DC-Link" solution: Terms for following sections.

Note: For simplification, the term "DC-Link" is used to refer to the entire solution comprising multiple xEVCap capacitors connected in parallel via a laminated busbar, including the external connections but excluding other systems such as power semiconductor modules and the battery. (Fig. 5)

Evaluation of parasitics at the system level

The primary parasitics of the DC-link, namely equivalent series resistance (ESR) and equivalent series inductance (ESL), significantly influence the overall system behavior. Accurately calculating these parameters during the design phase is challenging, particularly when using a component analyzer at higher frequencies. Instead, employing finite element modeling (FEM) electromagnetic

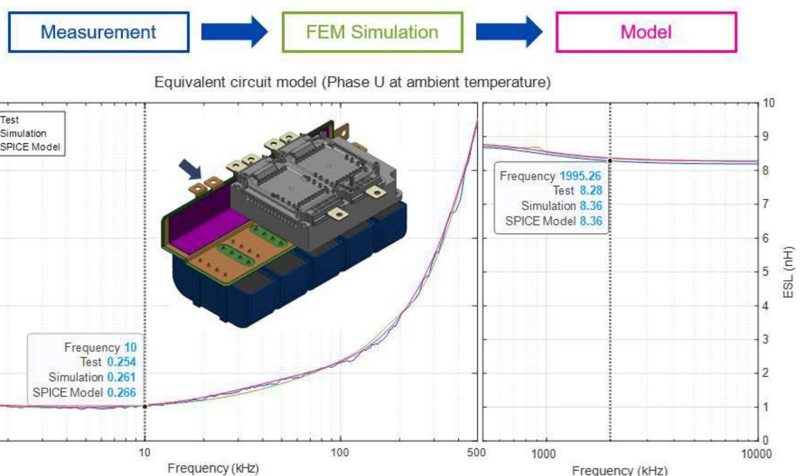


Figure 6. Virtual characterization process.

software facilitates a virtual characterization of the entire DC-link solution (including capacitance, ESL, ESR, and impedance). This characterization enables the development of reliable SPICE models, which allow for a more precise simulation of the converter's operation [11], as shown in Figure 6.

ESR (Equivalent series resistance)

The product of current squared and ESR ($I^2 \cdot ESR$) quantifies the power losses generated by the current flowing through the DC-link capacitors. The ESR is not constant but varies significantly with frequency. This frequency dependency directly affects the thermal losses within the system. Two current spectrums with identical RMS values but different frequency ranges will result in different power losses. This also applies to the distribution of these losses (i.e., where they are generated).

Figure 7 illustrates this concept: losses are calculated for the same automotive DC-link capacitor (with an identical ESR vs. frequency curve) and the same total capacitor current (in RMS). In one scenario, all current is applied at 10 kHz, while in the other, the current follows a typical automotive spectrum with a 10 kHz switching frequency at specified modulation parameters.

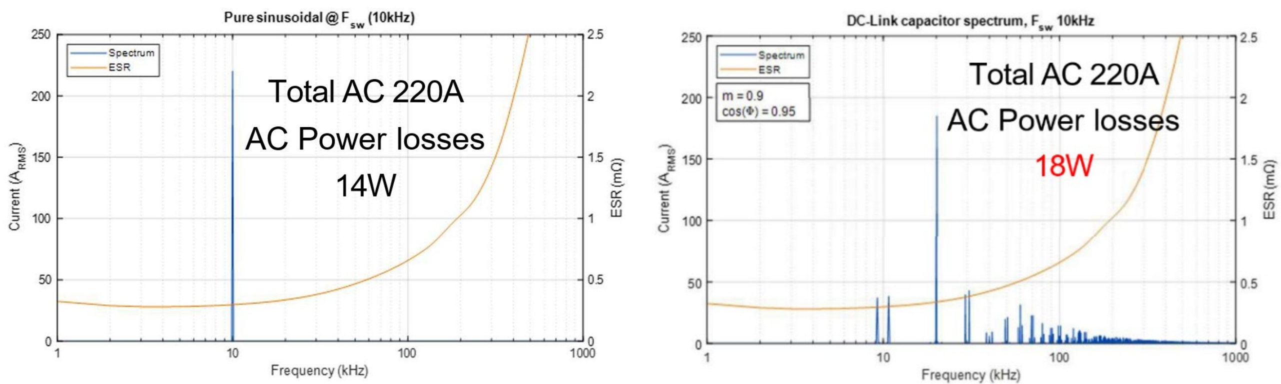


Figure 7. Comparison of the power losses in a DC-link capacitor under single frequency 10kHz (left), and under a realistic frequency current spectrum (right)

There are five primary reasons why ESR increases with frequency: skin effect, inhomogeneous impedance, internal resonances, negative electromagnetic interaction, winding geometry, and metal profile. xEVCap addresses the internal factors related to capacitor design. However, the design of the busbar and connections is crucial to mitigate inhomogeneous impedance, resonances, and negative electromagnetic interactions.

ESL (Equivalent series inductance)

To reduce the equivalent series inductance (ESL) of the DC-link, it is essential to understand the contribution of each component. It is a common misconception that the total ESL is simply the sum of the inductances of all its elements (capacitive elements, terminals, busbar, etc.). This assumption only applies to an ideal system without interactions between the elements. In reality, these interactions can either increase or decrease the system's ESL and must be evaluated on a case-by-case basis.

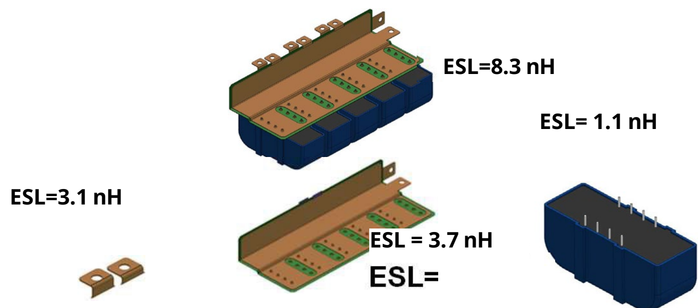


Figure 8. The sum of component inductances (7.9 nH) is less than the total characterized inductance (8.3 nH) due to interaction among the individual elements.

$$ESL_{DC-link} = \sum ESL_{parts} \pm \sum ESL_{interactions}$$

Figure 8 illustrates a DC-link composed of five xEVCap capacitors (B25654A8806K001, 80 µF, 850 V). The ESL is simulated at 2 MHz, resulting in a total inductance of 8.3 nH from the central pair of terminals. If all parts of the system are considered independently, the inductances are 3.1 nH for semiconductor terminals, 3.7 nH for the busbar, and 1.1 nH (5.4 nH/5) for the five capacitors in parallel. The sum of these independent components is 7.9 nH, which is lower than the total system inductance of 8.3 nH. This discrepancy arises because the different elements interact, increasing the total inductance by 0.4 nH. Therefore, while the method of directly summing element inductances can provide a rough and quick estimation, it is not highly accurate.

There are various strategies to reduce the inductance of the DC link based on the three sources of ESL in the system:

- Optimize the connection to the power modules to reduce the inductance of the terminals.
- Maximize the overlap in the busbar.
- Increase the number of capacitive elements (xEVCap) connected in parallel. Figure 9 (left) illustrates the improvement in ESL with an increased number of capacitive elements, together with the results of the double-pulse test with four capacitive elements.

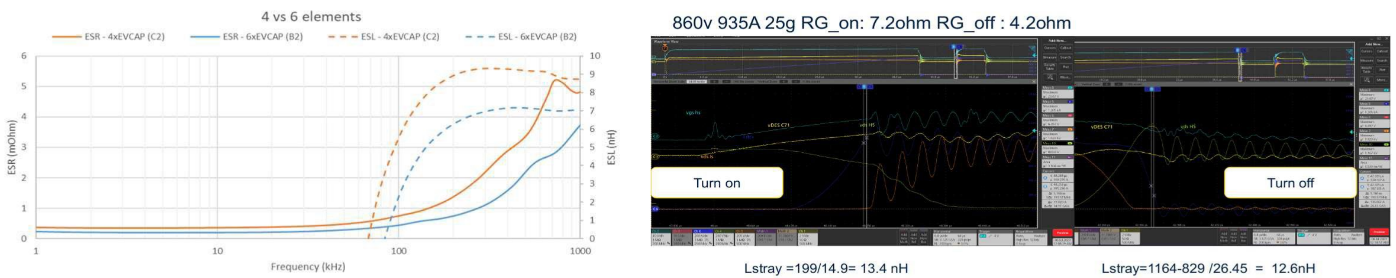


Figure 9. (Left). Simulation of ESR/ESL for a configuration 4 elements and 6 elements as per [1]. (Right) Double pulse test by STMicroelectronics (DSC Gemini 800 V/300 kW traction inverter). 4 x B25654A8137K002 (4x135 µF/850 V), showing a total stray inductance of 13 nH (all elements)

The total stray inductance measured in the double pulse test, as shown in Figure 9 (left), comprises all components: capacitors, busbars, and semiconductors. This measurement matches the simulation results presented in Figure 8 for the DC link, which includes capacitors, busbars, and terminals.

Joint technologies from elements to the busbar

The capacitor units should be connected in parallel via a laminated busbar, which then connects to the power semiconductors. While a printed circuit board (PCB) connection is another mounting option, it is not commonly used for the main power train inverter because a PCB can’t handle high currents. Each capacitor features eight round copper terminals (four for each polarity) with a diameter of 1.2 mm, plated with pure tin. Proper mounting requires a soldering process to ensure a reliable finish.

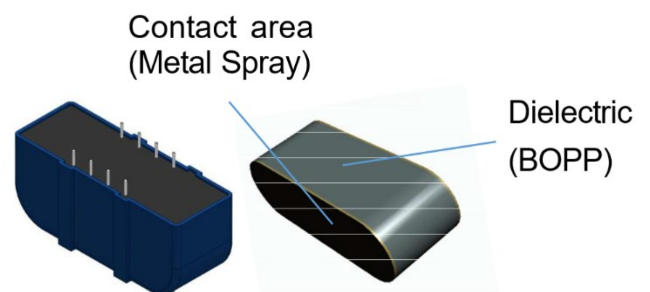


Figure 10. xEVCap and its internal capacitive element.

The soldering process will subject capacitors to certain thermal stress. Therefore, it is crucial to adhere to the cautions specified in the datasheet [9]. Exceeding the recommended temperatures can cause internal damage,

such as increased ESR due to issues in the electrode-film contact area, or decreased insulation resistance because the polypropylene dielectric was damaged (Fig. 10). For capacitors mounted on PCBs using the wave soldering method, the maximum body temperature must be controlled within the specified limits [9]: During pre-heating (T_p) lower than +110 °C; during soldering (T_s) lower than +120 °C, and time of soldering (t_s) lower than 45 seconds (Fig. 11).

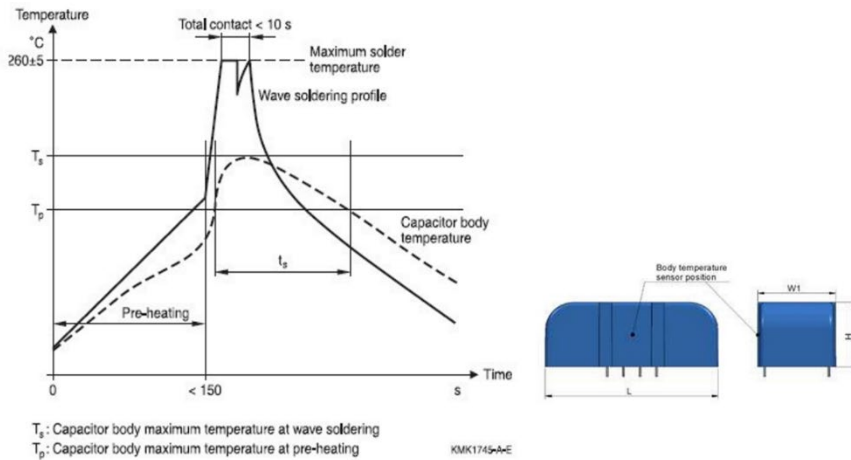


Figure 11. Extract from mounting guidelines of B25654A Datasheet [2].*

The laminated busbar

Rogers Corporation has more than 40 years of experience designing and manufacturing ROLINX laminated busbars. A laminated busbar is a multi-layer construction of conductors: copper or aluminum separated by thin dielectric materials, laminated in one structure. Electrically, it is a multilayer circuit that distributes the current from the capacitors (buffer) to the power modules (IGBT) through specific connections. In this sense, it is equivalent to a multi-layer PCB, but with the advantage of using much thicker conductors. This allows it to carry much higher currents. Typical currents in a busbar range from a few dozen amps to several hundred, even kiloamps for the thickest busbar conductors.

Parameter	Value
Voltage rating [V]	400 … 1,200
Peak voltage [V]	1600
I_{DC} or I_{AC} (cont.) [A]	60 … 500
Stray inductance [nH]	< 10 (depending on terminal design)
No. of capacitors	2 … 10+
Operating temperature (max.) [°C]	+105
Relative humidity (at +55 °C) [%]	95
Conductor material	Cu, Al
Plating	Sn, Ni
Insulation CTI [V]	≤ 600

Table 2. Typical values for ROLINX Caplink

Figure 12. Design example of three xEVCap (B25654A8137K001, 135 µF- with ROLINX CapLink. Collaboration between TDK and Rogers Corporation.

There are specific solutions for the EV market, one of which has been specially developed to integrate film capacitors such as TDK xEVCap: ROLINX CapLink. This range of busbars displays unique design to solder capacitors into ROLINX laminated busbars. The combined assembly is lightweight, extremely low inductive, and offers high power density. These characteristics make it especially suitable for SiC devices.

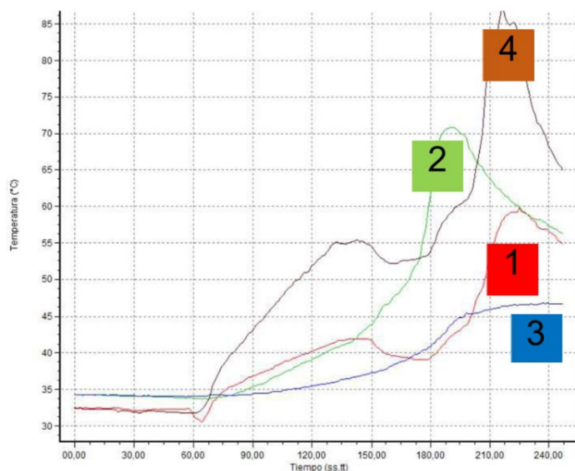
As they are fully custom-made, electrical ratings can be extended and designed to fit as many capacitors as required by the application. For reference, three xEVCap type C can be accommodated into a 17 x 17 cm CapLink with a busbar capable of carrying more than 400 A at 850 V.

Guidelines for soldering processes to laminated busbars

One of the approaches chosen by Rogers to integrate capacitors into a laminated busbar is a special busbar design that allows heat to concentrate around the soldering point, and performs a standard solder process: robot soldering, selective wave soldering, or wave soldering. Robot and selective wave soldering can be performed as described below. Wave soldering requires a protective mask to avoid damaging busbar insulation and to limit temperature rise during the process.

Figure 13. Details of selective wave soldering trials with the datalogger and probe position. Only bottom pre-heating, reaching a temperature of +60 °C on the busbar (bottom) in 75 s.

Rogers has experience in all the above-mentioned processes. Thanks to the special design of ROLINX CapLink around the soldering point, the busbar-to-capacitor solder process follows the same steps as standard pin soldering.



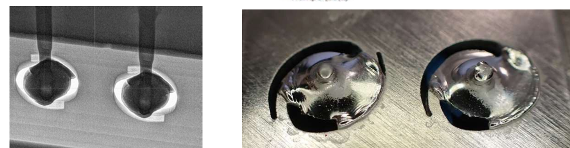


Figure 14. Temperature monitoring during soldering. Soldering quality

The selective wave soldering tests are conducted on an ERSA selective soldering machine, using SAC305 solder alloy and a crucible temperature of +290 °C (Fig. 13). The ROLINX module with the assembled capacitors can be passed directly through the machine without the need for mounting on any pallet/carrier.

For this experiment, since temperature profiles must be monitored, a universal pallet (not custom-made) is used to support the device and the data logger. It adds certain complexity because it makes it difficult to calculate the exact position of the pins to be soldered (XYZ). So, this complexity would not occur in the mass production process.

Figure 14 shows that, of the three probes placed on the capacitor, probe #2 reaches a slightly higher temperature (approximately +72 °C) near the soldering area. Probe #1 reaches about +59 °C, while probe #3 barely reaches +47 °C.

All temperatures are well below the specified soldering temperature of +120 °C, which is necessary to avoid damaging the capacitors.

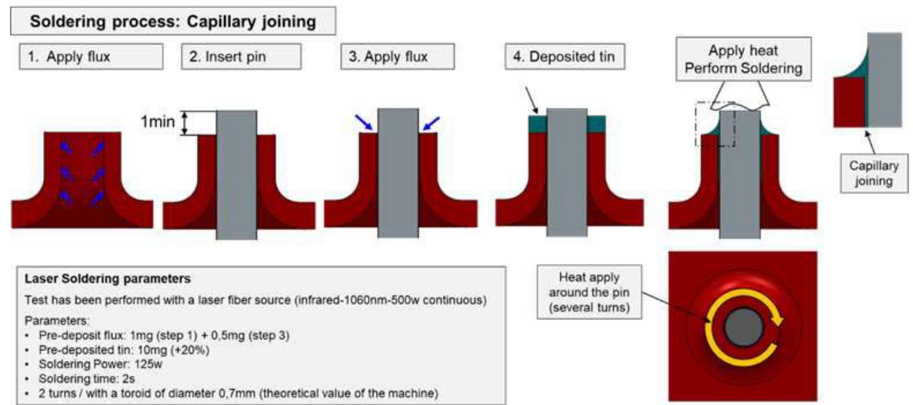


Figure 15. Illustration of the experiment in 5 steps performed for the soldering of xEVCap lead wire terminals

It is visually apparent that the soldering is correct with proper wetting. The small flux residues can be removed with brushing. These flux residues can also be minimized to be almost imperceptible by reducing the amount of flux used. (It is a matter of conducting more tests). The X-ray images also demonstrate that the solder has properly risen and formed a meniscus (cone) at the top.

Selective wave soldering is then feasible with proper wetting. The process time is the total soldering time for each lead (24 leads x 3.5 s + 0.7 s) plus the time for movements between leads. These times can be significantly reduced, as it may not be necessary to solder for such a long duration. It is a matter of conducting more trials. Also, for high volume, it is recommended to use a multi-wave solder module to solder all leads simultaneously.

Trials with laser soldering and a TDK busbar design

Selective soldering methods are recommended to prevent damage to insulators while ensuring efficiency, cleanliness, and a high-quality soldering finish. In this experiment, instead of using the Rogers CapLink busbar, a custom-designed stacked busbar connection for lead wires by TDK was utilized. A five-step laser soldering process is proposed in Figure 15 to minimize heat input and solder material, while achieving an optimal solder joint through capillary action.

The laser soldering equipment was specifically adapted for these trials with additional fixtures and custom programming. With two passes of the laser beam around the wire, there was no significant increase in

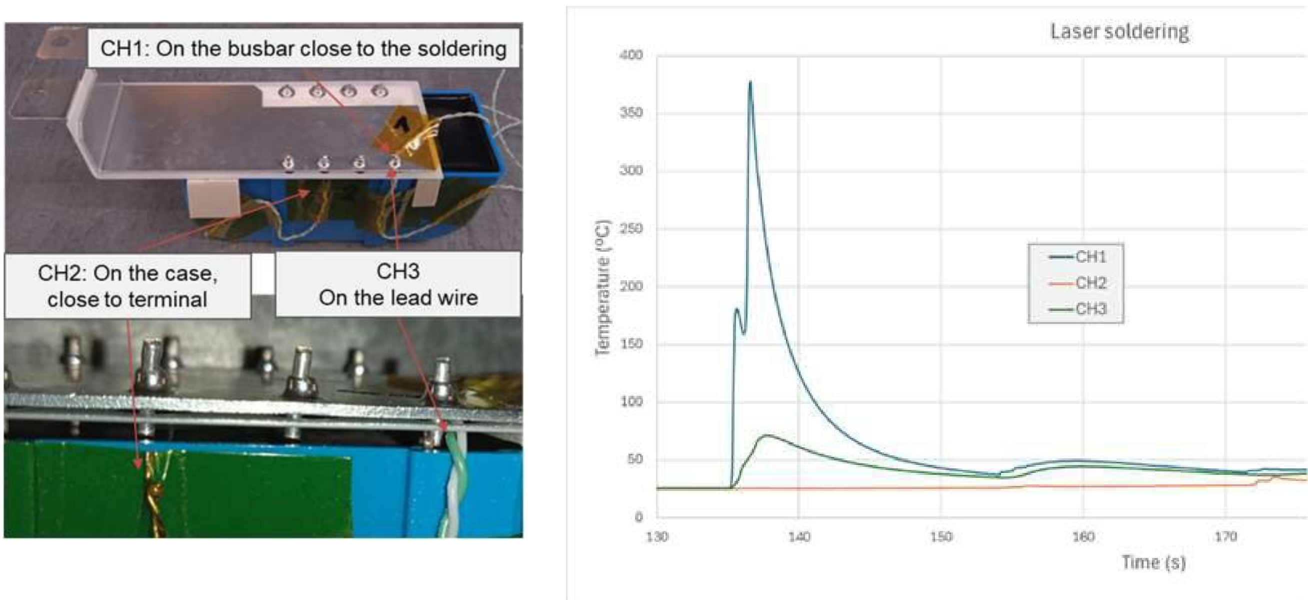


Figure 16. Temperature profiles in different areas. No relevant stress for the capacitor was observed

temperature on the capacitor body (CH2 in Fig. 16). Only the area to be soldered (CH1) was heated. The temperature was monitored in different areas. It was far below their maximum temperature ratings (Fig. 16).

The methodology involved trial and error until a stable soldering quality was achieved. Preliminary trials revealed issues such as gaps in the solder area or burnt tips and insulators, often due to manual tin-flux deposition control or excessive time and power. The primary challenge was that the laser equipment was not originally intended for this type of capillary soldering. The laser spot diameter had to be manually adjusted and was sometimes too wide during these trials.

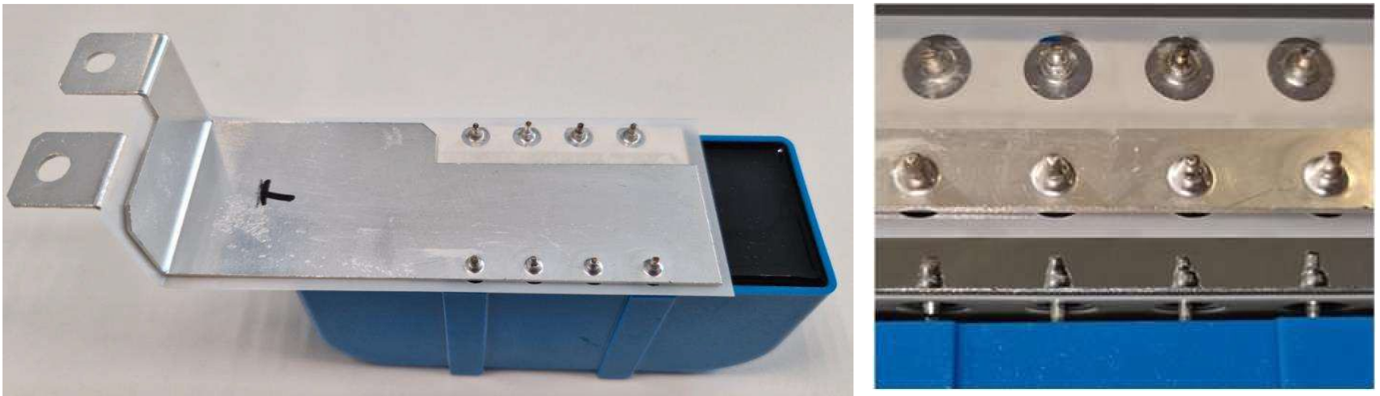


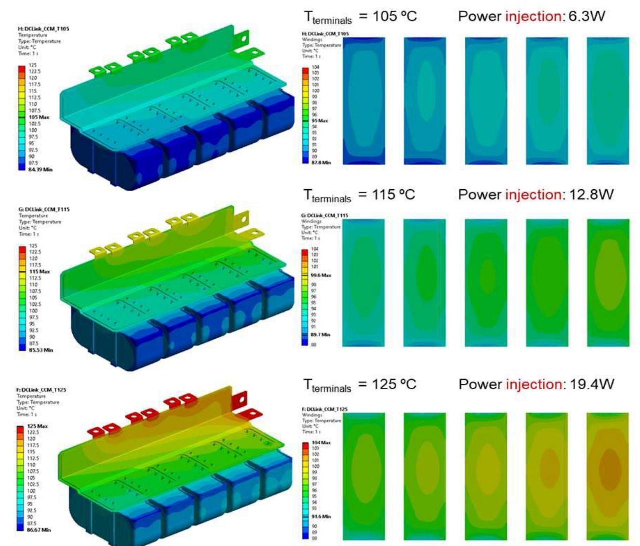
Figure 17. xEVCap with TDK's busbar design. After laboratory trials of the soldering process. Detail of terminals and finishes

For instance, reducing the power or spot diameter of the laser beam and slightly increasing the number of turns will promote a more homogeneous and progressive temperature distribution. This approach enhances capillary action and prevents burning of undesired areas, such as the tip and the insulator. Additionally, cutting the wire over the neck could contribute to tip burning due to chips. These aspects require further investigation and control to integrate this mounting process into mass production.

After several trials, the results were finally positive. A good soldering quality and a technically feasible process were achieved (Fig. 17). This means a smooth soldering appearance, good wetting, and no cold solder. The tin material completely fills the gap between the pin and the hole. There was no damage from the laser (due to excessive heating) to the plastic insulation or the pin, and no signs of burns.

Thermal integration and modelling

Following the study of parasitics on the system level and the joint technologies with the busbar, the next step is to evaluate the system from a thermal perspective, considering other elements such as the cooler and semiconductors. Thermal systems are complex to model and evaluate due to the high interactions between all



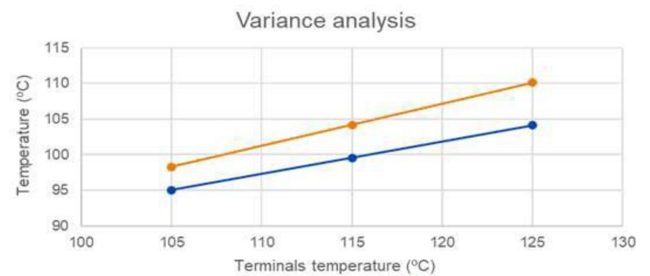


Figure 18. The importance of semiconductor terminal temperature. Thermal simulation with three temperatures at the terminals: +105 °C, +115 °C, and +125 °C. Cooperation between Infineon Technologies and TDK

components. For the automotive DC-link capacitor, the key aspects to consider are the terminal temperatures, the contact with cooling surfaces, and the capacitor hotspot temperature in the dielectric. This value defines the lifetime of the component under specified mission profiles or allowed voltage operation.

Influence of temperature on the terminals

The temperature at the capacitor terminals is the primary external thermal boundary condition, significantly influencing thermal behavior, aside from ambient temperature. The DC-link solution includes all connections to the semiconductors and the battery. These connections are thermally affected by the current flow corresponding to each operation mode of the inverter, as well as by the temperatures at the semiconductor and battery connections. Depending on these temperatures, power will flow from or to the DC-link (busbar and xEVCap) through these terminals, thereby extracting or injecting power losses.

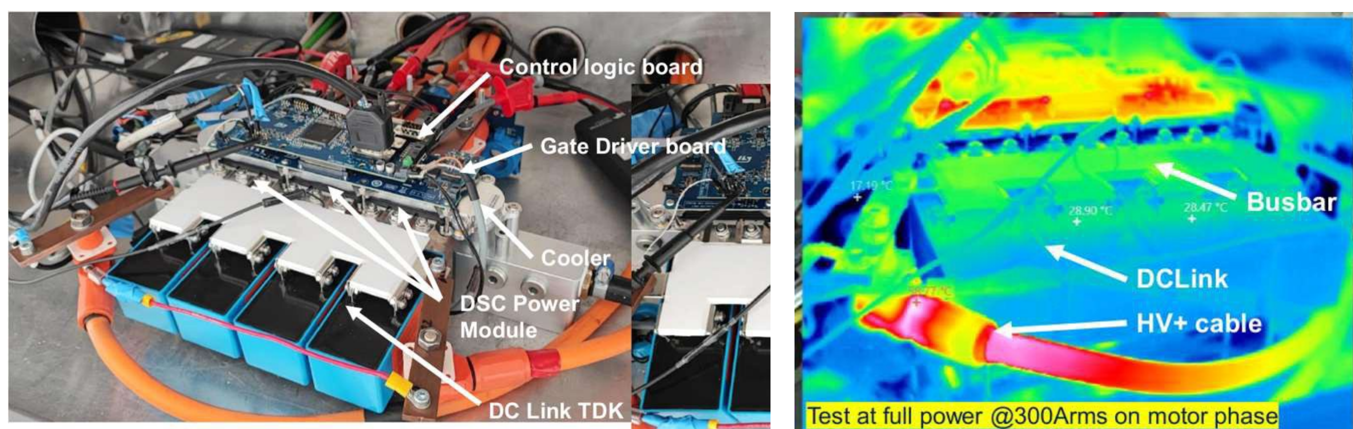


Figure 19. Infrared picture for 300kW Dual Side Cooling Traction inverter. Higher temperature on terminals. (courtesy of STMicroelectronics)

The terminals form a direct thermal path to the capacitive elements since the material used (copper) conducts heat very well and has a high cross-section. This significantly impacts the thermal behavior of the capacitor. The temperature of the dielectric (BOPP) will determine the maximum voltage and duration for which the capacitor can operate safely.

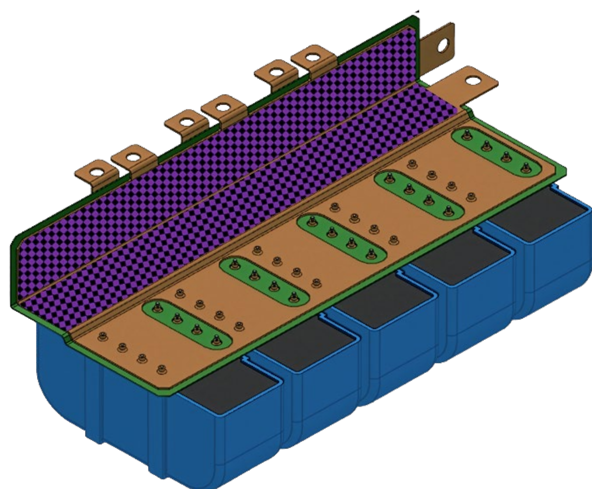


Figure 20. DC-link solution with thermopad (purple) in selected areas of the busbar to extract heat and decouple semiconductors and xEVCap thermally. Busbar design by Infineon Technologies AG.

To estimate the temperature distribution in the capacitor modules, these boundary conditions must be well defined. User specifications usually include the maximum temperature at the terminals for a specific mission profile. It should also be noted that this temperature depends on the operation mode and is affected by the cooling. The effect of terminal temperatures can be analyzed by running a series of thermal simulations, keeping all parameters constant except for the terminal temperatures.

Figure 18 shows the thermal results from simulations with capacitor losses of 35 W, applying DC battery current and AC current based on a given spectrum. The simulations were conducted with terminal temperatures set at +105 °C, +115 °C, and +125 °C, respectively. These results indicate that the system temperature is highly influenced by the terminal temperatures. Additionally, this boundary condition's effect is concentrated on the areas of the capacitor closest to the

semiconductor terminals. The xEVCap hotspot remains below these temperatures, as confirmed by subsequent real-world testing.

The semiconductor terminal temperature is a key boundary condition affecting capacitor temperatures and, consequently, its lifetime under defined mission profiles. It directly influences the capacitor hotspot and depends on the instantaneous power of the inverter. Some users specify the power flow through the terminals, providing a more accurate definition of the boundary conditions for simulation.

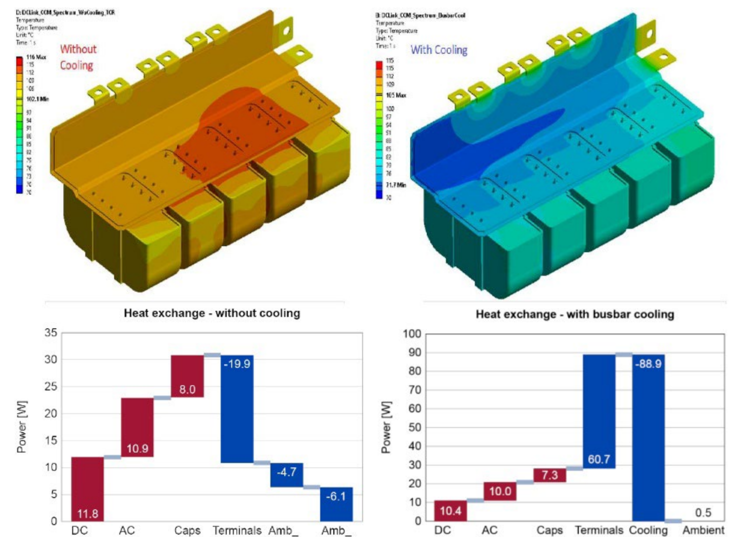


Figure 21. Simulation of a DC-Link solution under two different scenarios: without cooling (left) / with cooling (right). Cooperation between Infineon Technologies AG and TDK Red: Losses due to current. Blue: Boundary conditions. Positive: Injection into capacitors. Negative: Extraction

Active cooling influence on thermal behavior

The other external condition that directly impacts the temperature distribution inside the capacitor is active cooling. For most automotive DC-link applications, this is necessary due to the high requirements in terms of current and frequency, and due to the inherent poor natural cooling. The most used approach is water cooling with a closed-loop circuit.

The cooling block contacts the busbar (using a thermopad) on the marked areas (Fig. 20) as a suggested approach. The positioning of the cooling surface provides two benefits:

- Heat extraction: cooling area on the busbar in the most effective position. The high thermal conductivity of copper helps to remove not only the losses from the busbar but also from the xEVCap through its terminals.
- Thermal decoupling: A cooling surface located between the semiconductor terminals and xEV capacitors thermally decouples the DC link from the semiconductor modules (the biggest heat generator in the converter), reducing their influence on dielectric (BOPP) temperature.

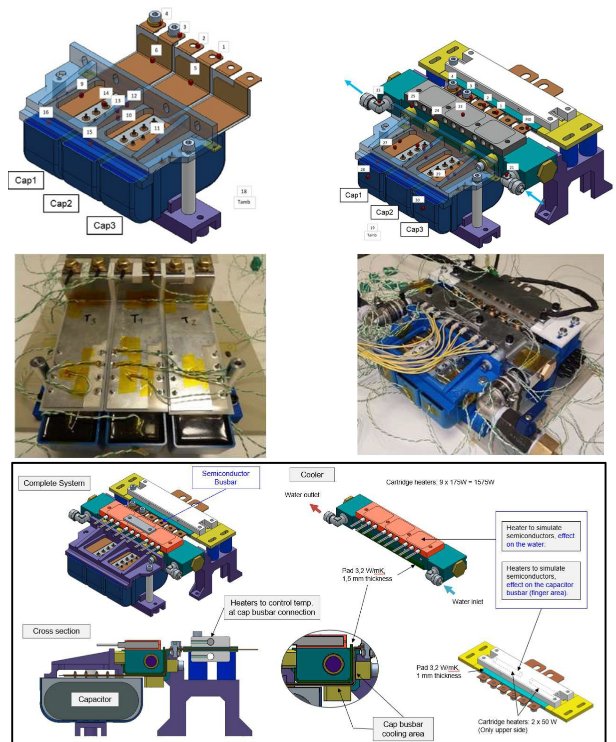


Figure 22. Illustration of the demonstrator setup for testing. One without a cooler (left) and the other with all the elements (heating and cooling) (right). Numbers indicate the position of the thermocouples.

Figure 21 shows the temperature distribution in the DC-link solution with and without active cooling, and a heat exchange analysis showing the heat inputs and outputs of the complete system (power losses with boundary conditions). When the system is not cooled (Figure 21, left), the maximum temperature increases. The heat generated by the capacitors is not adequately dissipated, leading to overheating of the capacitor dielectric. This heat becomes trapped between the semiconductors and capacitors. When cooling is applied (Fig. 21, right), the hottest spots of the system are the semiconductor terminals, and all the heat is extracted through the cooler. This is why this type of cooling is preferred for automotive applications.

When possible, the active cooling surface should be over the copper surfaces and located between the semiconductor terminals and the capacitive elements to decouple the temperature of the capacitor dielectric from the temperature of the semiconductor terminals.

Thermal integration in the demonstrator

For this purpose, a demonstrator (Fig. 22) for laboratory testing has been developed according to the specifications required by automotive converters.

It aims to demonstrate the thermal integration with a cooler and how the different elements interact under different heating/cooling conditions. The construction includes three xEVCaps (B25654A8806K001 80 µF/850 V; 56 A (RMS)) with a nominal power capability of approximately 150 kW. It is integrated into a system with a removable cooler and heater to simulate the losses of the power semiconductors.

Two different setups have been tested under predefined electrical conditions (168 A (RMS) at 20 kHz) at ambient temperature: One setup without external cooling or heating (Fig. 22 left) and the other setup with all the elements (heating and cooling, Fig. 22 right).

To simulate the power losses of the semiconductor (approx. 1500 W), nine cartridge heaters, each rated at 175 W, were placed over the cooler, replicating the positions of the semiconductors. Additionally, two more resistors were added at the connection with the busbar to reproduce the heat transferred by the semiconductor terminals, thereby maintaining the temperature at the semiconductor terminals. To ensure good thermal contact and maximize the heat extracted by the cooler from the busbar, a thermal pad of 3,2 W/(m·K) and a thickness of 1.5 mm is used over the cooling area.

A test matrix has been elaborated by varying the conditions of the water inlet temperature (+50 °C or +60 °C), the water flow rate (5 L/min or 8 L/min), and the temperature in the connection between the busbar and the semiconductors (ranging from +70 °C to +100 °C):

<table>
<tr><th>Test</th><th>AC frequency [kHz]</th><th>Water temperature [°C]</th><th>Busbar (semiconductor) temperature [°C]</th><th>Water flow rate [L/min]</th><th>Active cooling</th></tr>
<tr><td>1a</td><td rowspan="2">20</td><td>Without cooler</td><td>Not controlled</td><td>N/A</td><td>N</td></tr>
<tr><td>1b</td><td>50</td><td>70</td><td>8</td><td>Y</td></tr>
<tr><td>2a</td><td rowspan="5">20</td><td>50</td><td>80</td><td rowspan="4">8</td><td>Y</td></tr>
<tr><td>2b</td><td rowspan="3">60</td><td>80</td><td>Y</td></tr>
<tr><td>2c</td><td>90</td><td>Y</td></tr>
<tr><td>2d</td><td>100</td><td>Y</td></tr>
<tr><td>2e</td><td>60</td><td>80</td><td>5</td><td>Y</td></tr>
</table>

Table 3. Test matrix for thermal testing

The test results (Fig. 23) indicate a thermal decoupling between the capacitors and the heaters (which emulate semiconductor temperatures). The system effectively extracts heat from the capacitors, as the temperature of the busbar area in contact with the cooler is lower than the hottest point measured on the capacitors.

In the first setup (without a cooler and no busbar heating, Fig. 22 left), the busbar temperature is about +55 °C, and the maximum temperature of +62.1 °C is observed in the case between capacitors (thermocouple 17). In the second setup (case 2E, with the whole integrated system with water temperature of about +60 to +64 °C and heater at +135 °C), the highest temperature is detected in the xEVCap terminals with a value of +85.7 °C.
The laser soldering connections between the xEVCap terminals and the busbar have shown good behavior during the test, without significant overheating detected compared to the busbar plate (1,7 K in the worst case).

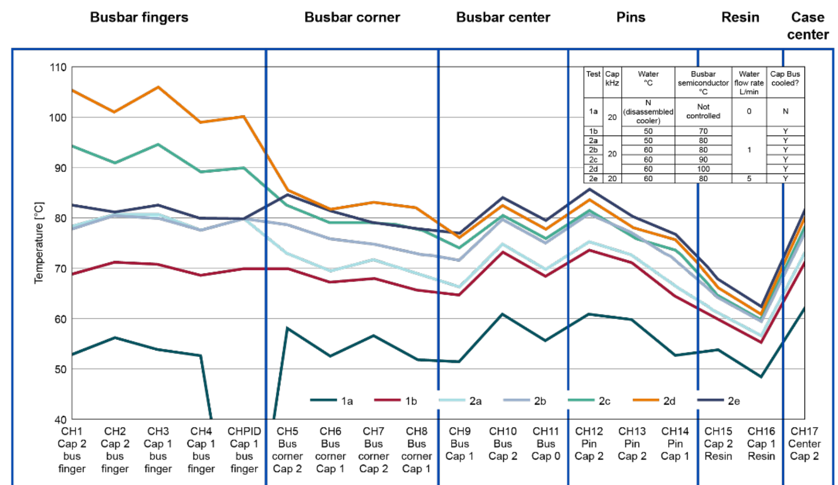
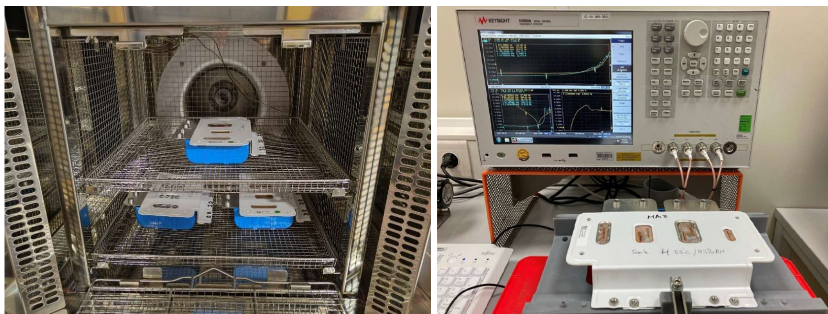


Figure 23. Temperature results applying 168 A (RMS) of the test conditions defined in Table III. Channel location is indicated in Fig. 22

The conditions tested may not exactly match the specifications required by automotive converters, but these results will help designers better understand thermal distribution and optimize cooling strategies.



Frequency	At 1 kHz		At 10 kHz		At 100 kHz	
Parameter	**C_S [µF]**	**R_S [µΩ]**	**C_S [µF]**	**R_S [µΩ]**	**C_S [µF]**	**R_S [µΩ]**
Before	415.2	264.4	586.7	599.1	–	–
After	414.6	296.2	627.5	740.7	413.3	496.6
Before	413.6	258.2	622.8	607.7	–	–
After	412.8	287.4	610.9	744.9	411.6	581.5
Before	415.3	278.0	562.1	603.2	–	–
After	414.9	281.8	622.5	777.2	413.5	535.4

Figure 24. Testing snapshots: Humidity bias, thermal cycles (by Rogers Corporation), and electrical characterization.

Conclusion

xEVCap offers an alternative DC-link solution for traction inverter power designers compared to traditional custom solutions. Custom solutions require high-volume demand for industrialization, whereas xEVCap is an off-the-shelf solution. This approach is uncommon for traction inverter designers but is widely used in lower power electronics with printed circuit boards, product catalogs featuring multiple ratings, voltages, and dimensions. The same philosophy is applied to xEVCap, providing all necessary design information online.

Additional design aspects have been reviewed, including system-level parameters, busbar design, assembly technologies, and thermal strategies, focusing on the interaction between elements from a thermal perspective. These aspects are supported by advanced simulation tools, real-world testing in a demonstrator, and collaboration with leading companies in power semiconductors and busbars.

Future Work

For joint technologies, mass production will always require process optimization, control, and cycle time reduction. For laser soldering, the tin wire can incorporate flux, and automation of preform insertion or auto-feeding the tin wire. Laser soldering methods can be used for SMD film capacitors, which would otherwise need larger and more expensive dielectrics and enclosures to be compatible with standard SMT reflow processes. Additionally, energy consumption, factory area, cleanliness, quality, process control, and yield are other variables that need to be investigated to support the incorporation of these new selective soldering processes for mounting electronic components.

A full set of testing is being conducted on the assembly: Visual inspection of soldering, electrical characterization, damp heat, humidity-bias voltage, thermal shock test, high operating life test, thermal stability, and vibration (Fig. 25).

For the demonstrator, the next step is virtual characterization to develop accurate models of complete systems with thermal behavior under various power and cooling scenarios. Regarding the product, future investigations will focus on aspects such as miniaturization and integration with other components (e.g., EMC filter).

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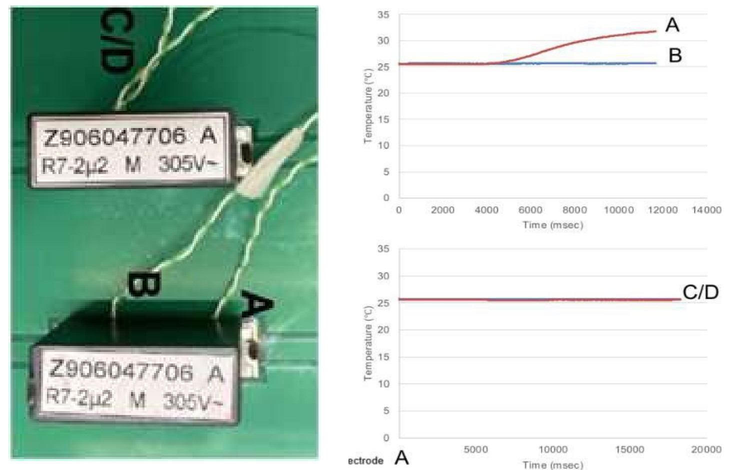

Figure 25. Detail of temperature profile for laser soldering to an SMD film capacitor (X2- 2.2 µF/305 V (AC)). Laser soldering process applied to SMD film capacitors by Hamamatsu Photonics [12]

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