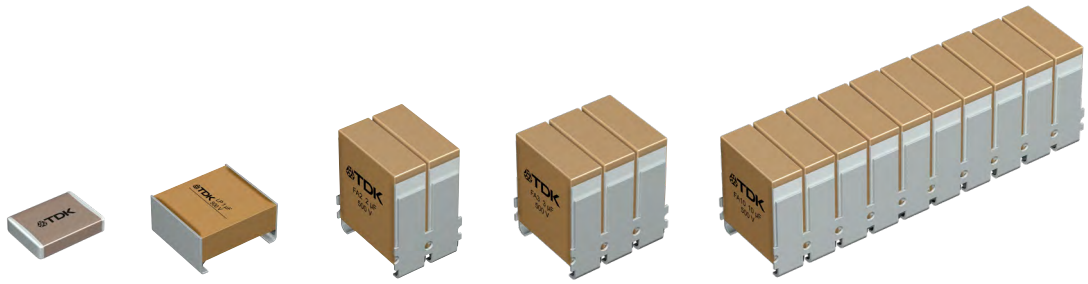
TECHNICAL GUIDE 2026

CeraLink Capacitors



Product details
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General remark

This document is a guideline for engineers working with CeraLink. CeraLink is a PLZT (lead lanthanum zirconium titanate) based ceramic capacitor with antiferroelectric behavior, which is optimized for high-frequency and high-temperature power electronic applications.

We exemplify this using figures and values of CeraLink LP 500 V series (P/N B58031I/U5105M 62), unless otherwise mentioned. Electrical characterization values for this type are:

$V_{pk,\ max}$	V_R	V_{op}	$C_{nom,\ typ}$	$C_{eff,\ typ}$	C_0
650 V	500 V	400 V	1 µF	0.6 µF	0.35 µF ±20%

Table 1: Technical parameters for CeraLink LP 500 V

The main features of CeraLink are:

- Increasing capacitance with DC bias between 0 V and V_{op} and best in class capacitance density at operating point (V_{op} & T_{op})
- High current capability due to low losses at high frequencies (up to several MHz) and high temperatures (up to +150 °C)
- Designed for high dV/dt ratios, i.e., suitable for fast switching, respectively, high switching frequencies (e.g., SiC or GaN applications)
- Good thermal self-regulating properties
- Qualification based on AEC-Q200
- RoHS-compatible PLZT ceramic (see RoHS exemption 7(c)-II). For detailed information, please refer to the TDK_Environmental Protection Website.

CeraLink is not recommended for operation under constant polarity change (AC voltage) due to increased self-heating induced by re-poling losses – please see chapter >Polarization< for details.

Capacitance

CeraLink features a non-linear capacitance behavior, i.e., the capacitance strongly depends on external parameters such as the applied DC bias voltage or the temperature. It is important to note that CeraLink is designed to have its maximum capacitance under operating conditions, where we distinguish two scenarios:

1. DC-link operation, i.e., operation under a DC bias (constant operating voltage) and with a superimposed ripple amplitude. As explained in the following, for this scenario, it depends on the amplitude of the superimposed ripple voltage, whether the effective capacitance C_{eff} or the nominal capacitance C_{nom} should be considered.*

2. Snubbering/filtering, i.e., operation to filter out voltage spikes. These voltage spikes can be superimposed on a specific DC bias voltage, for example, the characteristic voltage spikes that are superimposed on the operating voltage during fast semiconductor switching, as shown in Figure 1, or the voltage spikes are induced by fast current switching of an inductive load, e.g., when disconnecting an electric motor or pump from the battery supply in a protection circuit. In this case, the voltage may start from 0 V to some peak voltage.

In all these scenarios, the applied current is limited only indirectly by the maximally rated device temperature of +150 °C, where we note that operation above rated temperature is possible in principle but not recommended since it will affect the lifetime of the capacitor.

*We note that the full nominal capacitance C_{nom} can be achieved only if the voltage seen by the CeraLink capacitor spans a sufficiently large range in the hysteresis loop as explained in section >Measurement of C_{nom} (nominal capacitance)<. This is typically fulfilled in a snubber application, where for DC link applications, it is usually not the case such that in this case a capacitance in a range between C_{eff} and C_{nom} can be obtained realistically. The exact value depends on the superimposed ripple amplitude. Further details will be provided in section >Capacitance Calculation<.

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Furthermore, the induced voltage spikes must not exceed the maximally allowed peak voltage $V_{pk,max}$ for a given CeraLink type, i.e., short voltage pulses ranging from 0 V to $V_{pk,max}$ are tolerable, and there is no limit on dV/dt, respectively, dV/dt is limited by the intrinsic ESR of the capacitor.

Usually, in all these scenarios, values close to the nominal capacitance C_{nom} can be considered. This is also commonly referred to as the large signal capacity. Details about the definition and how to measure the large signal capacitance are explained in section >Measurement of C_{nom} (nominal capacitance)< .

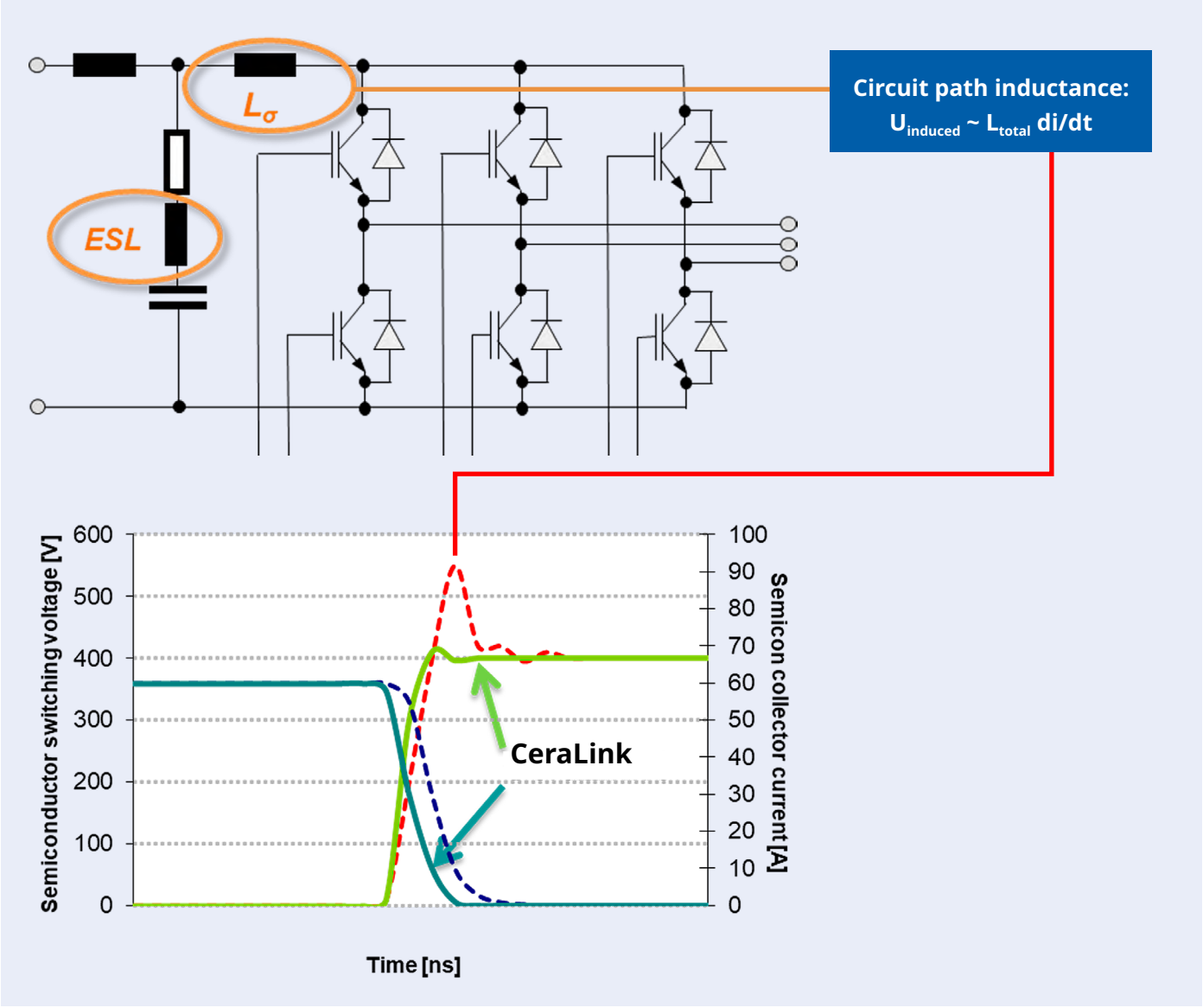

Figure 1: Semiconductor overshoot principle. The larger the overall inductance, the higher the voltage spikes induced during switching. With a high temperature rating of +150 °C, CeraLink capacitors can be placed close to semiconductor devices, thereby minimizing the overall commutation loop inductance.

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Note that the specific operating voltage V_{op} for all CeraLink types is usually 100 V below the rated voltage V_R, i.e., in case of the LP 500 V, the operating voltage is 400 V. This is also the regime in which the device provides maximal capacitance.

Due to this intrinsic non-linearity, there are usually three different capacitance values stated in the CeraLink data sheets: the initial capacitance C_0, the effective capacitance C_{eff}, and the nominal capacitance C_{nom}, where the latter value defines the rated capacitance of a CeraLink capacitor:

- **Initial capacitance C_0:** measured at 0 V DC, 0.5 V AC (RMS), 1 kHz, room temperature
  This means no DC bias and just a small AC voltage is applied. (This measurement corresponds to a usual incoming inspection test with an LCR meter.)

- **Effective capacitance C_{eff}:** measured at operating voltage V_{op}, 0.5 V DC, V AC (RMS), 1 kHz, room temperature
  Same as the C_0 measurement but with a DC bias (constant operating voltage), which is, in this case, the operating voltage V_{op}. This measurement corresponds to the usual operation under DC-link voltage with a small, superimposed ripple amplitude. Throughout, this will be also denoted as the small signal capacitance.

- **Nominal capacitance C_{nom}:** measured at operating voltage V_{op}, quasistatic, room temperature
  The nominal capacitance value is derived from the maximum of the mean hysteresis through the common definition C = dQ/dV. Throughout, this will be also denoted as the large signal capacitance. The measurement is explained in the chapter >Measurement of C_{nom} (nominal capacitance)< .

These definitions, together with the corresponding voltage scenarios, are schematically depicted in Figure 2.

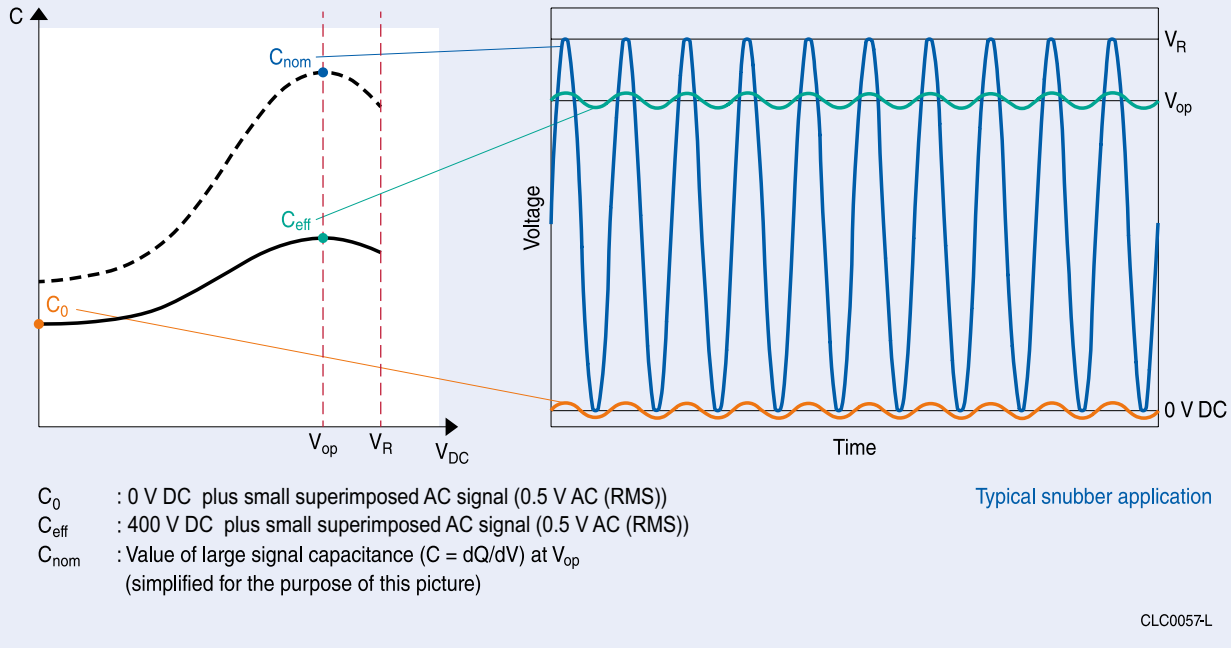

Figure 2: (left) Schematic representation of capacitance versus DC bias for small signal (solid line) and large signal (dashed line), as well as definition of the capacitance values C_0, C_{eff}, and C_{nom}. Note that the maxima of C_{eff} and C_{nom} do not necessarily coincide; instead, they may be slightly shifted with respect to the operating voltage V_{op}. (right) Schematic representation of corresponding voltage levels. The definition of small and large signals depends on the applied voltage waveform. For small, superimposed ripple amplitudes (small signal), the effective capacitance C_{eff} should be considered. In contrast, for very large voltage amplitudes (large signal), the nominal capacitance C_{nom} is typically applicable.

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Physical background

Antiferroelectric (AFE) materials offer distinct advantages for energy storage applications, particularly in pulsed power systems, due to their unique physical properties. A key advantage of these materials is their ability to store and release energy through a field-induced phase transition from the AFE to the ferroelectric (FE) state. This transition involves a significant change in polarization, which enables efficient and reversible energy cycling.
In contrast, conventional dielectrics rely solely on capacitive storage. In addition, they exhibit low dielectric losses and maintain high efficiency even under fast charging and discharging conditions.

Their capacity to withstand high electric fields further increases the usable energy per unit volume, making them good candidates for advanced energy storage technologies.

The following table compares the dielectric behavior of representative ceramic materials. The shaded areas illustrate recoverable electrostatic energy density, where larger areas correspond to better energy storage performance. The width of the hysteresis loop reflects energy losses during charging and discharging; therefore, narrower loops indicate higher efficiency.

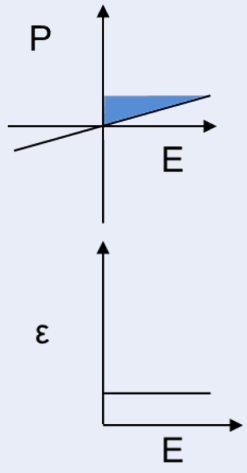
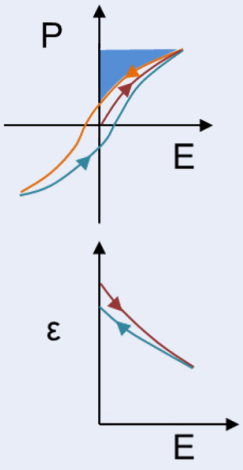
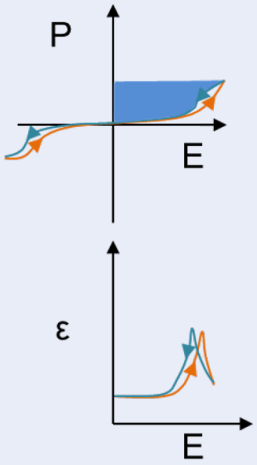
	Linear	Ferroelectric	Antiferroelectric
			
Nature of electrical polarization	Electronic, ionic	Permanent dipoles form ferroelectric domains	Permanent dipoles form antiparallel domains
Material class	(Ba,Nd)TiO, typ. NP0, COG	$BaTiO_3$ (BTO), typ. X7R	$(Pb,La)(Zr,Ti)O_3$ (PLZT)
Advantages	ε constant over electric field and temperature	ε up to 10,000 is possible	ε increases with field
Disadvantages	ε < 100	ε decreases strongly with electrical field	ε low at zero bias

Table 2: P = dielectric polarization, E = electrical field strength, ε = permittivity

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Physical background

As previously discussed, AFE materials utilize the reversible phase transition between the non-polar AFE phase and the polar FE phase to store and release energy. These two phases differ in the orientation of their dipole moments within the domain structure, as shown schematically in Figure 3.

In contrast, the transition between the paraelectric (PE) phase – present above the critical temperature T_c – and the AFE phase typically occurs during thermal processing, such as reflow. Above T_c, the material exhibits PE behavior, while below T_c, it adopts the AFE phase.

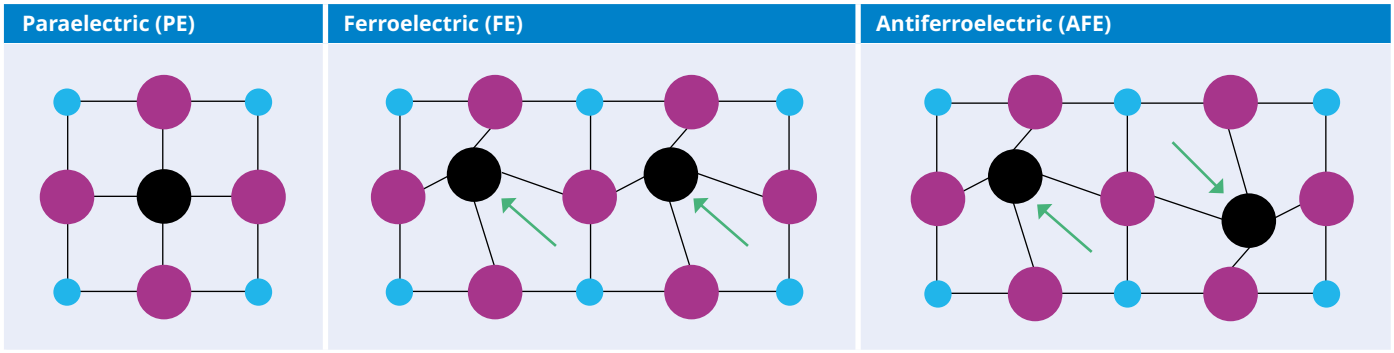

Figure 3: Schematic representation of paraelectric, ferroelectric, and antiferroelectric states. Taken from Randall CA, Fan Z, Reaney I, Chen L-Q, Trolier-McKinstry S. Antiferroelectrics: History, fundamentals, crystal chemistry, crystal structures, size effects, and applications. J Am Ceram Soc. 2021;104:3775–3810. https://doi.org/10.1111/jace.17834

During the AFE phase, the dipoles are arranged in an antiparallel configuration. This results in a non-polar state, where individual dipole moments cancel each other out, yielding a net dipole moment of zero. When a sufficiently strong external electric field is applied, these dipoles reorient and align with the field, inducing a transition to the FE phase with a net polarization across the domains, where a narrow hysteresis loop is essential for minimizing energy losses during charging and discharging cycles (see Figure 6 in section C_{nom}-measurement for a typical hysteresis of CeraLink). The permittivity (or capacitance) is defined as the derivative of polarization with respect to the electric field, or equivalently, the derivative of charge Q with respect to voltage U. This is schematically depicted in Figure 4.

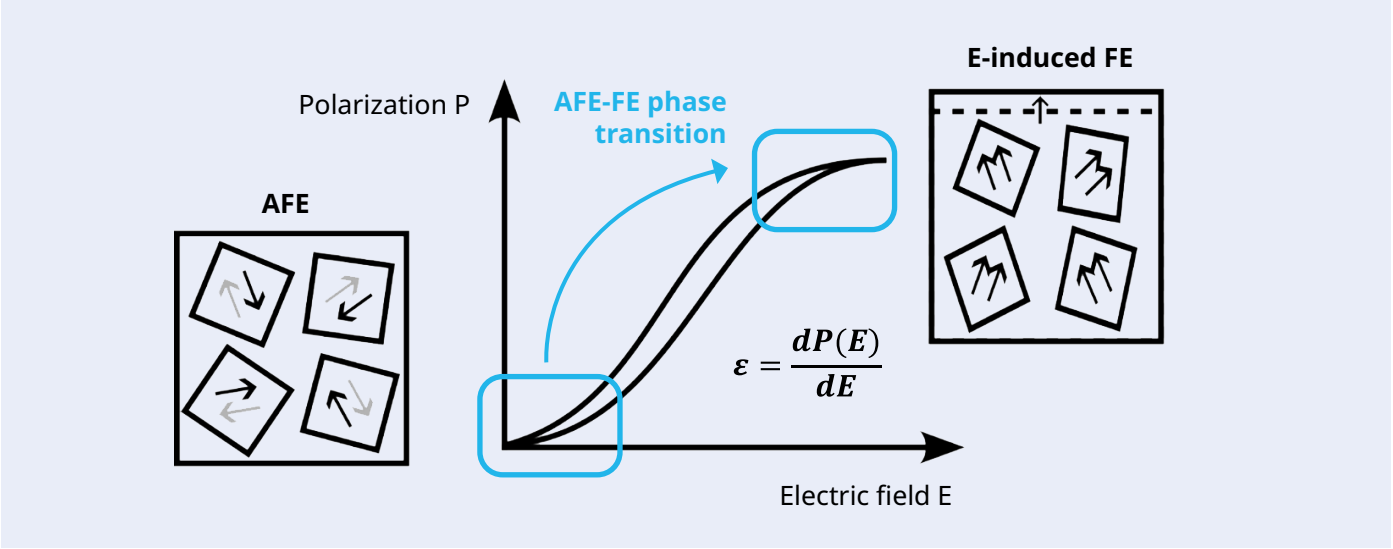

Figure 4: Schematic representation of the antiferroelectric (AFE) to ferroelectric (FE) phase transition. Note that the permittivity (or capacitance) is derived via the derivative of the hysteresis loop with respect to the electric field, or equivalently, the derivative of charge with respect to voltage.

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Measurement of C_0 (initial capacitance) and C_{eff} (effective capacitance)

The initial capacitance C_0 of CeraLink is defined using the following conditions: only a negligible external field is applied. That means that C_0 is measured at zero DC bias voltage and with a small sinusoidal AC field of 0.5 V (RMS) at 1 kHz oscillator frequency at room temperature (small signal).

On the other hand, the effective capacitance C_{eff} is defined under the same conditions, but with a defined DC bias applied. This means that C_{eff} is measured at operating voltage V_{op} with a small sinusoidal external field of 0.5 V (RMS) at 1 kHz oscillator frequency at room temperature (small signal).

Measurement of C_{nom} (nominal capacitance)

The base is a quasi-static unipolar polarization measurement, where the electrical charge on the capacitor is monitored versus the voltage. The capacitance is then obtained from the derivative.

$$C(V) = \frac{dQ}{dV}$$

The term “quasi-static” indicates that the voltage level is increased slowly enough to ensure that the resulting charging current remains below the maximum current capability of the measurement device. Since this limit depends on the specific equipment used, the permissible rate of voltage change may vary. In this context, a dV/dt range of 100 to 500 V/s is generally appropriate and will not affect the measurement outcome, provided the equipment can supply the corresponding current.

For the measurement, the voltage is ramped up/down according to:

$$V(t) = k \cdot t$$

The triangular function should be selected in such a way that k = 100 ... 500 and the maximum applied voltage is set to a value equal or slightly below to $V_{pk,max}$ for the applicable CeraLink type as specified in the data sheet.

The described measurement procedure and the polarization curve Q(V) are shown in the following diagrams:

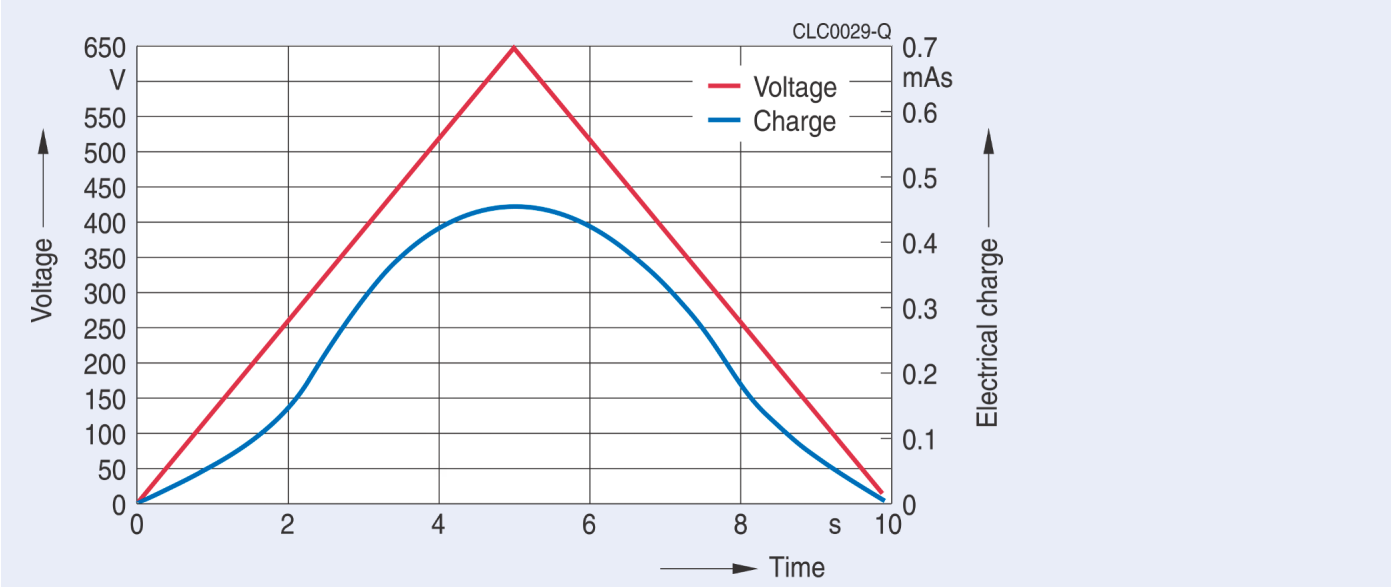

Figure 5: Electrical charge and voltage versus time.

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Measurement of C_{nom} (nominal capacitance)

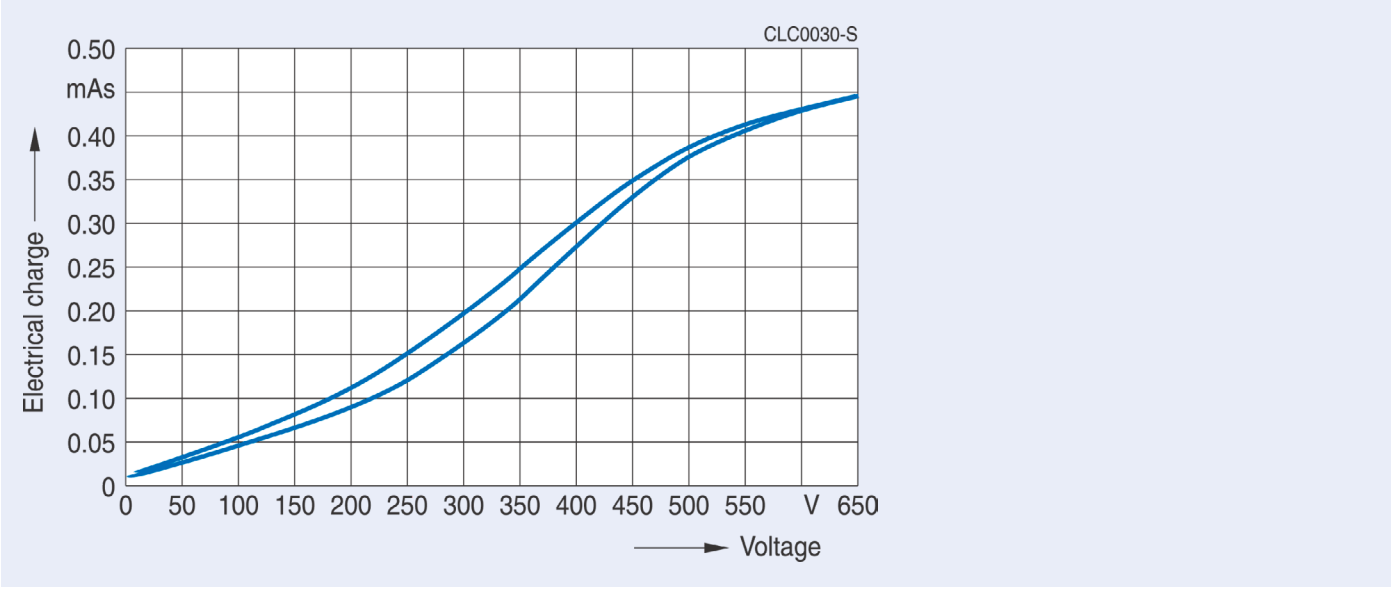

Figure 6: Electric charge versus voltage. Note that the electric charge will differ for each type of CeraLink (in this case, it is for a CeraLink LP 500 V capacitor).

As stated previously, the differential capacitance is defined as the derivative of the electrical charge with respect to the voltage, i.e. applying the derivative to the polarization curve shown in Figure 6 results in the following capacitance diagram (Figure 7):

In a final step, the average between the two blue envelope curves is taken. Here, the value of the curve at operating voltage V_{op} corresponds to the nominal capacitance C_{nom} as defined in the data sheet. This value corresponds roughly to the maximum of the curve, or phrased differently, the capacitance maximum of a CeraLink is centered around its respective operating voltage V_{op}.

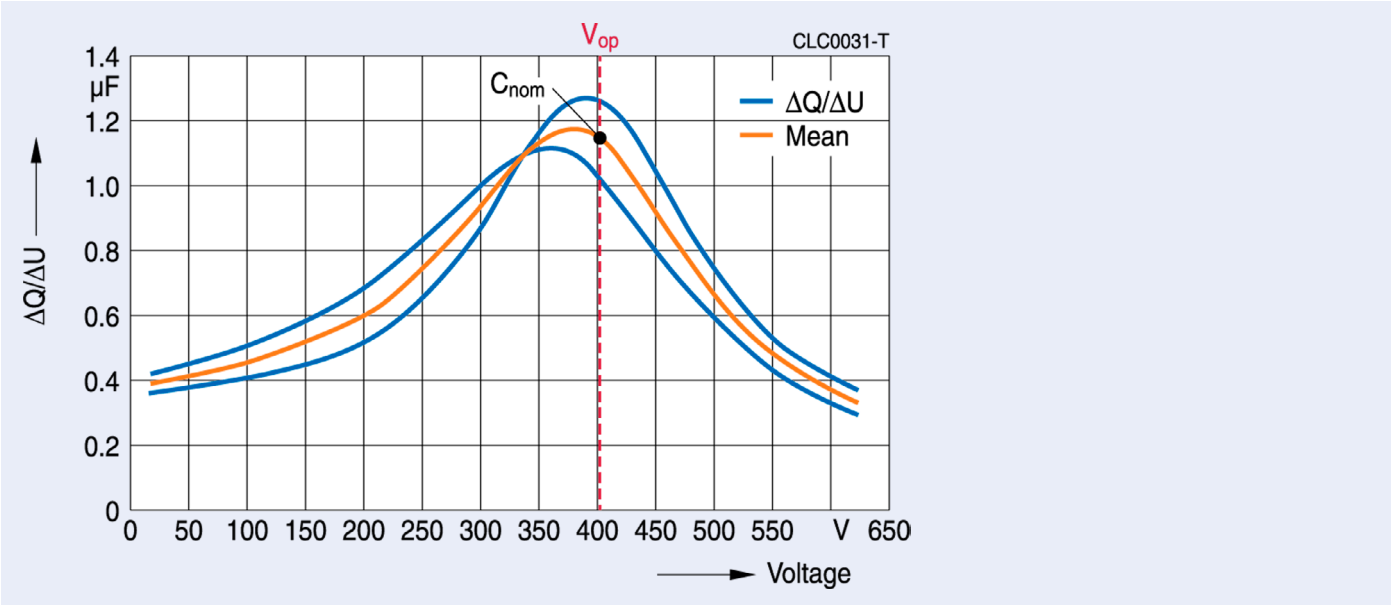

Figure 7: Derivative of the hysteresis Q(U) shown in Figure 6. C_{nom} corresponds to the value of the mean curve at V_{op}.

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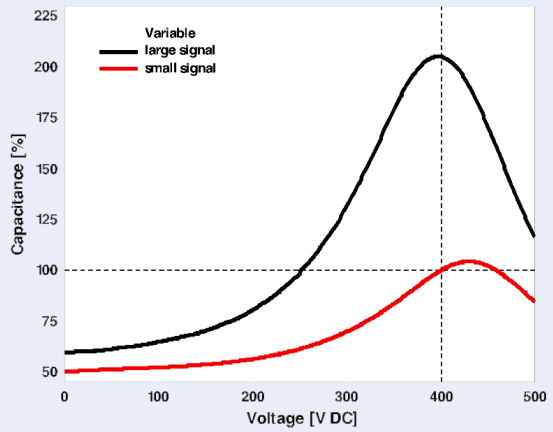
Measurement of C_{nom} (nominal capacitance)

Figure 8 illustrates the difference between the small-signal capacitance and the large-signal capacitance of a CeraLink at room temperature.



Small signal capacitance (**red curve**).
The effective capacitance C_{eff} corresponds to the value at
V_{op} = 400 V DC.

Large signal capacitance (**black curve**).
The nominal capacitance C_{nom} corresponds to the value at
V_{op} = 400 V DC.

Figure 8: Capacitance measurement at large and small signal for CeraLink LP 500 V. Note that the exact location of the capacitance maxima also depends on the device temperature, as discussed in the next section. The 100% value corresponds to $C_{eff,typ}$ as defined in the data sheet (see Table 1 in this document for an example).

Temperature dependence of capacitance

The capacitance of CeraLink depends on the applied voltage (DC bias), superimposed ripple amplitude, frequency, and ambient temperature. While the frequency dependence is typically small (see section >Frequency Dependence of Capacitance<), the temperature dependence is significant, as illustrated in the following figures, and should be taken into account in the application.

Note that these non-linear properties of CeraLink are implemented in our simulation tool, which is available on our website: www.tdk-electronics.tdk.com. The tool includes several LTspice model libraries covering most CeraLink types. It is designed to support engineers in selecting and integrating the appropriate CeraLink component into their application more easily.

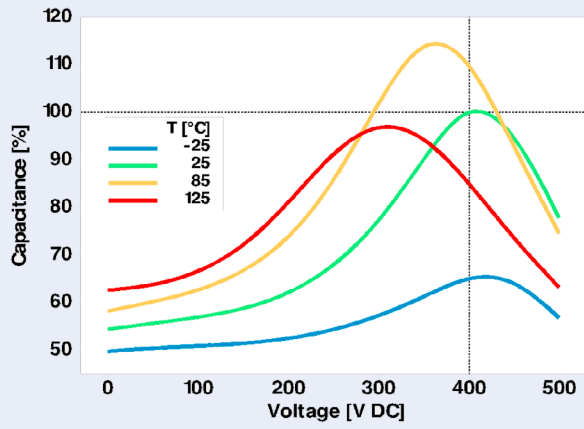


Figure 9: Voltage dependence of capacitance for different temperatures. The 100% value corresponds to $C_{eff,\ typ}$ as defined in the data sheet (see Table 1 in this document for an example).

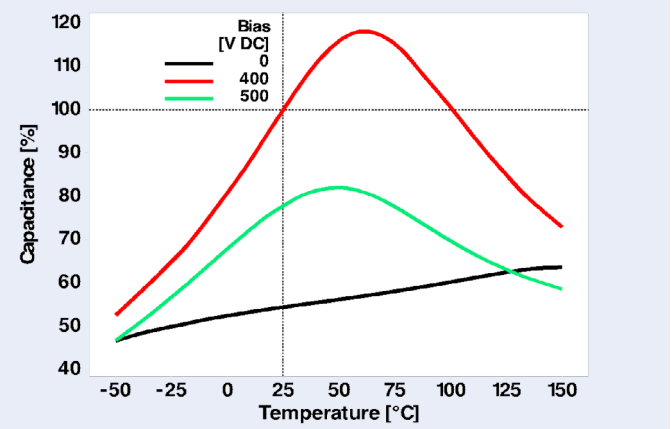


Figure 10: Temperature dependence of capacitance for different DC bias voltages. The 100% value corresponds to $C_{eff,\ typ}$ as defined in the data sheet (see Table 1 in this document for an example).

Capacitance

Temperature dependence of capacitance

At the operating voltage, the capacitance reaches its maximum at approximately +60 °C, meaning the optimal temperature range for CeraLink at V_{op} is +50 to +90 °C. It is important to note that at lower temperatures – particularly below +25 °C – the device may heat up more quickly compared to other ceramic capacitors (e.g., C0G or X7R) as it approaches its optimal working point. This “feel-good” temperature can be significantly higher than the ambient temperature and results from the increased ESR at low temperatures, as illustrated in Figure 12.

Due to its low losses at high temperatures, CeraLink is capable of handling higher currents under elevated thermal conditions.

At the same time, the capacitance decreases with increasing temperature, resulting in strong self-regulating thermal characteristics. As a result, the component carrying the highest temperature draws reduced current, thereby avoiding localized hotspots and minimizing the likelihood of thermal runaway.

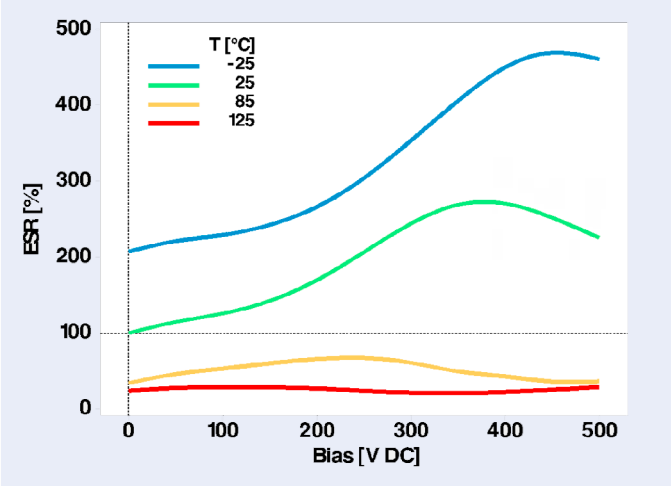


Figure 11: DC bias dependence of ESR for different temperatures. The 100% value corresponds to the typical ESR value as defined in the data sheet (i.e., typical ESR at 0 V and 0.5 V AC ripple at 1 kHz, room temperature)

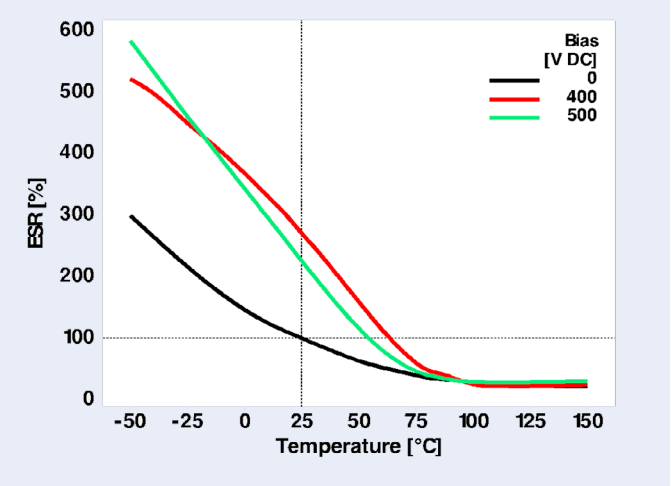


Figure 12: Temperature dependence of ESR for different DC bias voltages. The 100% value corresponds to the typical ESR value as defined in the data sheet (i.e., typical ESR at 0 V and 0.5 V AC ripple at 1 kHz, room temperature)

In Figure 13, the temperature dependence of the effective capacitance C_{eff} and the nominal capacitance C_{nom} is shown. As discussed previously, C_{eff} and C_{nom} correspond to the small-signal capacitance (small AC ripple) and the large-signal capacitance (voltage signal spans full voltage range), respectively. Both values are evaluated at the operating voltage V_{op}, which in this case is 400 V DC. Note that C_{nom} does not exhibit the significant temperature drop in the low temperature range that is observed for C_{eff}. Above an operating temperature of approximately +70 °C, the dependence of the effective capacitance on the AC ripple becomes weaker, and the two capacitance values begin to converge.

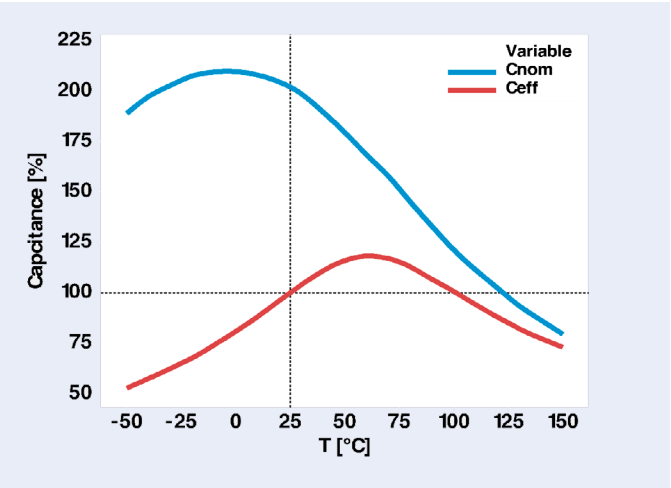


Figure 13: Typical nominal capacitance C_{nom} versus typical effective capacitance C_{eff} for different temperatures for a CeraLink LP 500 V. The 100% value corresponds to $C_{eff,typ}$ as defined in the data sheet (see Table 1 in this document for an example).

Capacitance

Temperature dependence of capacitance

Furthermore, it is important to note that CeraLink is optimized for high switching frequencies. At lower frequencies (below 10 kHz), the ESR and impedance increase significantly, as shown in Figure 14.

Optimal ESR values occur in the frequency range of 100 kHz to several MHz at room temperature. However, as shown in Figure 12, the effective ESR decreases by several orders of magnitude at a typical application temperature of +75 °C and above.

As previously noted, the maximum applicable dV/dt ratio is fundamentally limited only by the intrinsic ESR of the capacitor. The same principle applies to short-peak current pulses, which are in principle limited by two factors:

1. the overall induced voltage on the capacitor must stay below $V_{pk,max}$, and
2. the induced device temperature stays within the rated limit.

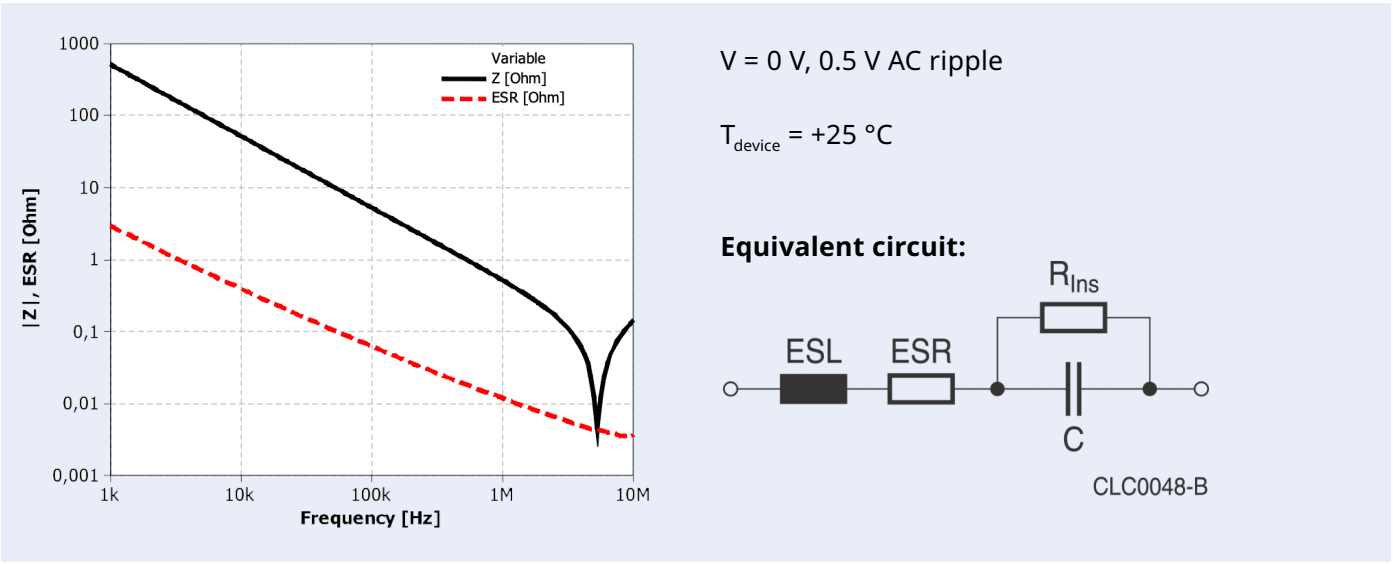


Figure 14: Impedance curve of CeraLink LP 500 V

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Frequency dependence of capacitance

The frequency dependence of the small signal capacitance (C_0) is shown in Figure 15. Up to the resonance frequency at around 5 MHz, the capacitance is relatively constant.

Typical deviations of up to -3% in the frequency range from 1 kHz to 1 MHz can be expected.

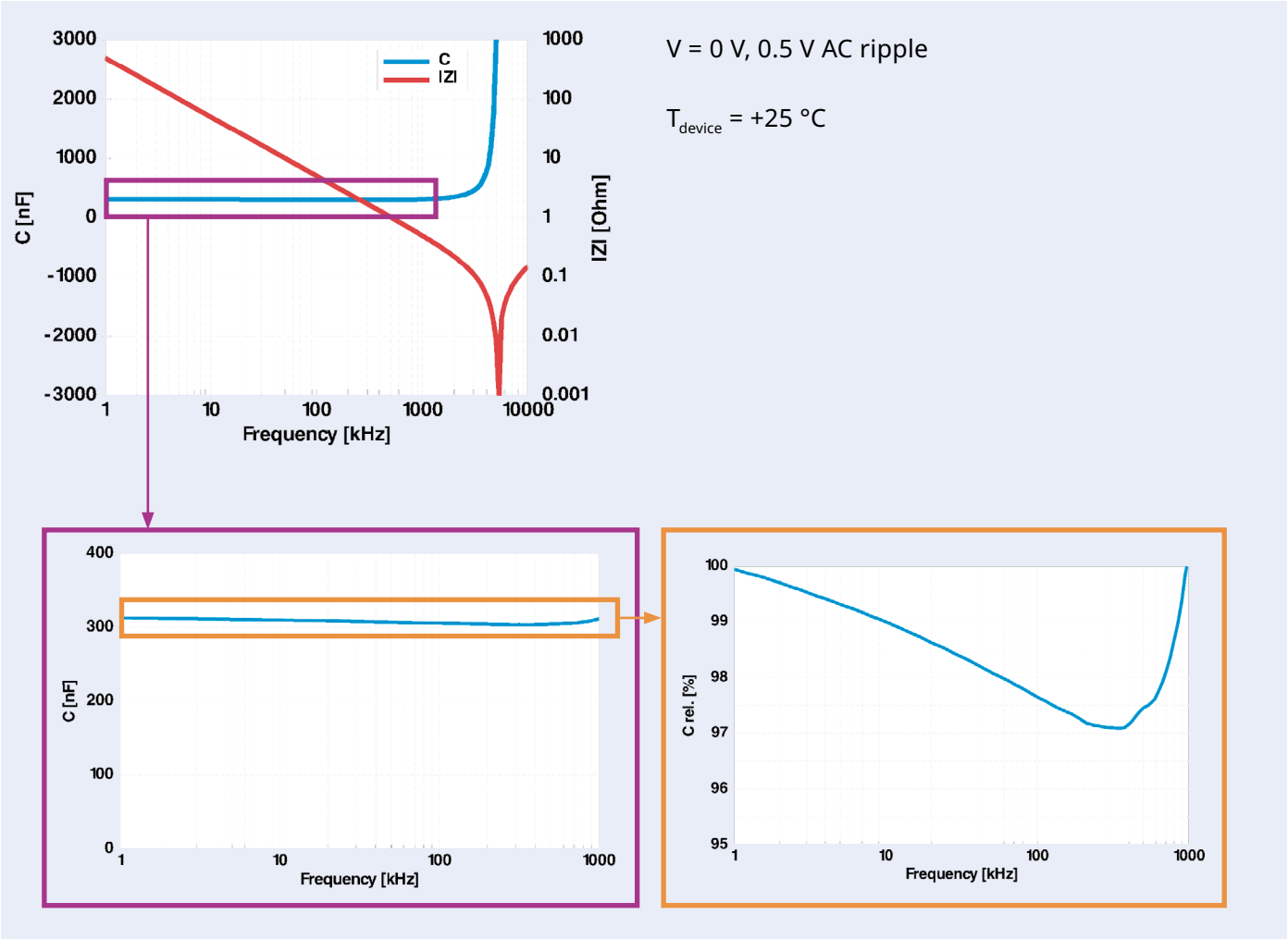

Figure 15: Frequency dependence of small signal capacitance C_0 of CeraLink LP 500 V.

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Capacitance

Capacitance calculation

In the following example, we consider a CeraLink LP 500 V, which has a typical effective capacitance $C_{eff,typ}$ = 600 nF. The application conditions are:

$V_{DC\ bias}$ = 350 V, f_{ripple} = 50 kHz, T_{device} = +115 °C.

Note that it is not relevant whether the device temperature is caused by self-heating or by ambient temperature, i.e., it could be T_{amb} = +80 °C and ΔT = 35 K, resulting in T_{device} = +115 °C.

Furthermore, we consider the three scenarios with

1. a small, superimposed ripple voltage (0.5 V AC (RMS)) – see green curve below
2. an intermediate superimposed ripple voltage (20 V AC (RMS)) – see red curve below
3. a large signal (voltage signal covers full voltage range) – see blue curve below

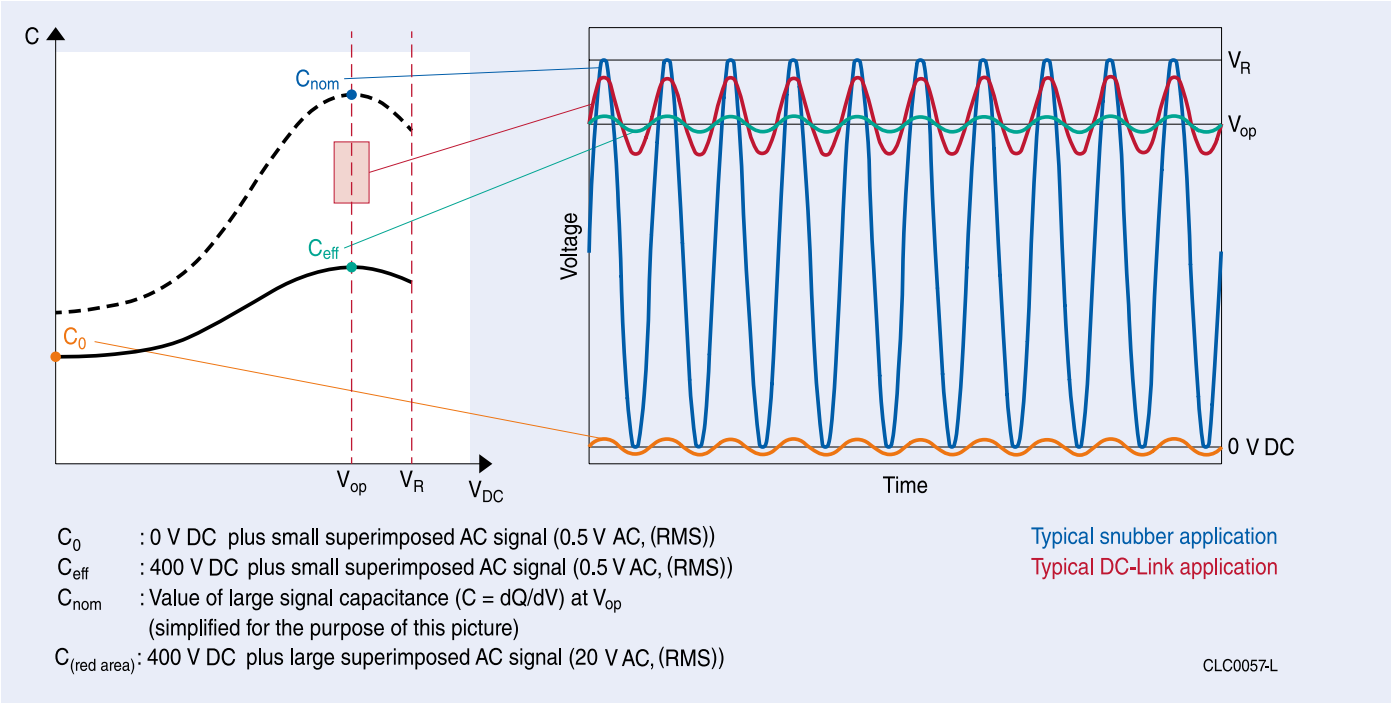

Figure 16: Small signal scenario (green), intermediate signal scenario (red), and large signal scenario (blue) for our calculation example.

Capacitance

Capacitance calculation

From the capacitance graphs in the CeraLink LP 500 V data sheet (see Figure 17), the effective capacitance at a DC bias of 350 V and 25 °C is approximately 90%, i.e., about 10% lower than the value at 400 V (see green curve). Considering the temperature dependent capacitance increase, the data indicate values of 114% at +85 °C (orange curve) and 95% at +125 °C (red curve). Linear interpolation between these two values yields an estimated value of approximately 109% at +115 °C, corresponding to an increase of about 9% relative to the nominal effective capacitance C_{eff} of 600 nF.

As shown in Figure 15, the capacitance exhibits a frequency-dependent variation of approximately -2% within the relevant frequency range. Taking all effects into account, the overall capacitance change is approximately +7%. Accordingly, the resulting capacitance for the small signal scenario 1 under these operating conditions is about 640 nF.
In contrast, the capacitance for the intermediate-signal scenario 2 increases to approximately 700 nF (about 10% higher). For scenario 3, the capacitance rises to roughly 750 nF (about 17% higher), as illustrated in Figure 18.

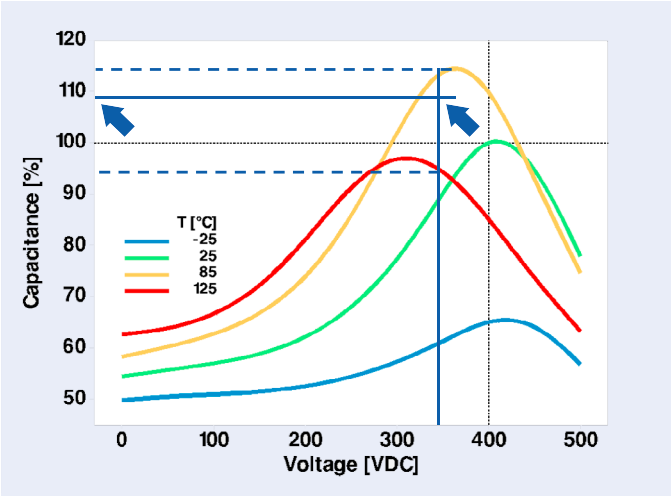

Figure 17: Relative capacitance values for different operating conditions.

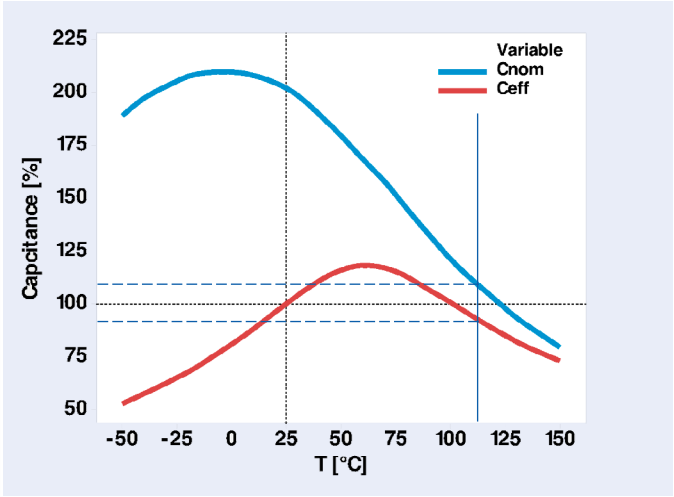

Figure 18: Difference between C_{eff} and C_{nom} over different operating temperatures.

Please note that this calculational example is intended only to illustrate the non-linear behavior of CeraLink capacitors. For a more detailed analysis tailored to specific application conditions, please refer to the simulation tools available on our website: www.tdk-electronics.tdk.com.

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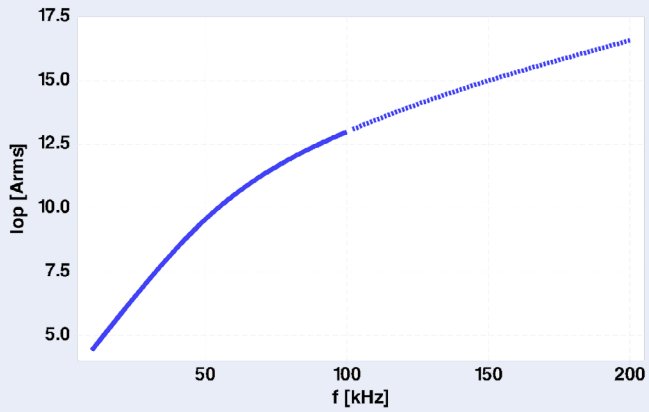
Current capability

CeraLink is optimized for operation at high frequencies and elevated temperatures. As shown in Figure 12, the ESR decreases significantly under these operating conditions. Consequently, both efficiency and current capability improve when the device is operated in this regime. This behavior is also evident in Figure 19, which illustrates the current capability of a CeraLink LP 500 V at different frequencies.

When increasing the switching frequency from 100 kHz to 200 kHz, the current capability rises by approximately 33%; from 200 kHz to 400 kHz, it increases by an additional 28% and from 400 kHz to 800 kHz by a further 24%. All values shown represent worst-case conditions, i.e., operation without any applied cooling. The corresponding experimental setup is described in the following.



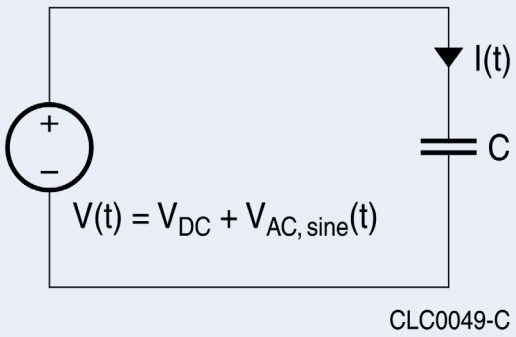
$T_{ambient}$ = +85 °C

T_{device} = +150 °C

The capacitor is mounted on a standard FR4 PCB without a heatsink and no forced airflow.

Figure 19: Current capability of a CeraLink LP 500 V for different frequencies.

The current capability is measured using the setup shown in Figure 20.



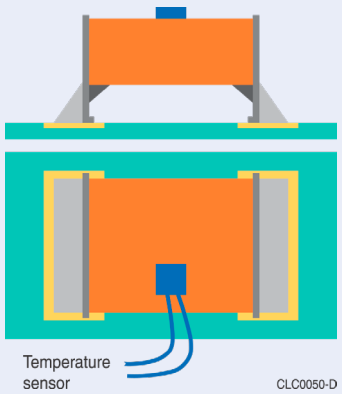


Figure 20: Schematic circuit for the current capability measurements. The device temperature is measured using a standard PT100 probe that is glued directly to the ceramics.

Using a fixed DC-bias voltage of V_{op}, the superimposed sinusoidal ripple voltage amplitude $V_{AC,sine}(t)$ is iteratively adjusted so that the resulting current drives the device to a predefined operating temperature (e.g., +150 °C). The temperature of the device is measured using a temperature sensor, which is attached to the top side of the ceramics.

We note that the primary heat dissipation path in CeraLink occurs through thermal conduction via the copper inner electrodes and the terminations (lead frames) into the PCB. Only a fraction of the heat is removed by convection to the surrounding air. Consequently, an effective cooling concept, i.e., efficient mounting to a heatsink, is essential for maximizing the current-carrying capability of the device.

Current capability

Figure 21 schematically illustrates this concept. In the first scenario, the device is mounted only on a PCB without any additional cooling (i.e., no heatsink and no forced airflow). This configuration is used for our data sheet measurements, as it represents the worst-case operating condition. In the second scenario, the device is mounted on the same PCB, but with an added aluminum heatsink and forced airflow*. Under these enhanced cooling conditions, the current capability increases significantly. At 10 kHz and 100 kHz, the improvement is approximately 54% and 33%, respectively.

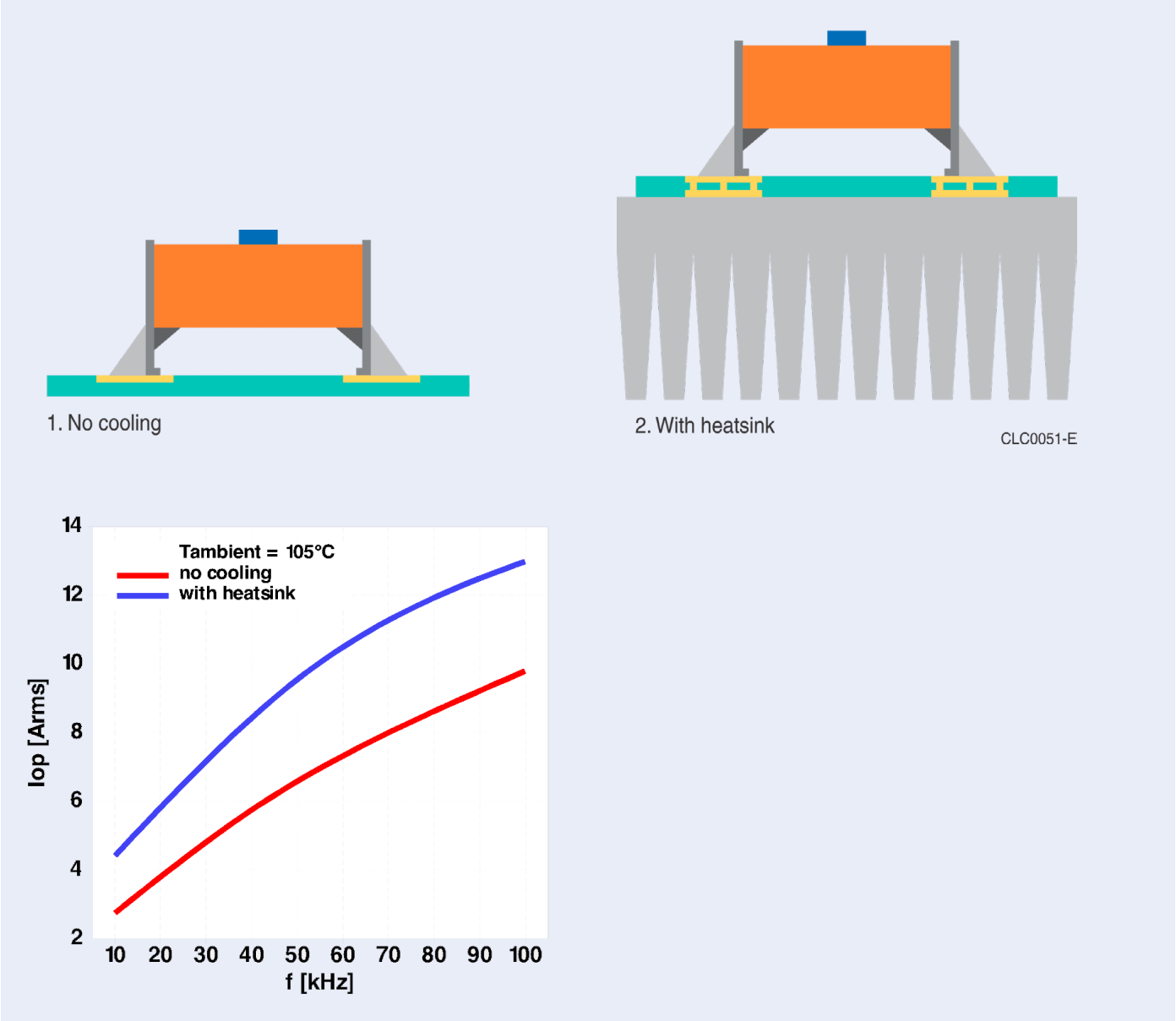


Figure 21: Current capability of CeraLink LP 500 V using two different cooling setups.

* Throughout this experiment, a standard 40 x 75 x 100 mm aluminum heatsink was used, providing a thermal resistance of approximately 1.2 to 1.4 K/W. For safety reasons, the heatsink was electrically isolated from the PCB using a layer of Kapton® foil. Forced airflow was supplied by the oven fan. It should be emphasized that this example is intended only to illustrate the importance of an appropriate cooling concept. The achievable current capability in an actual application may differ, as it depends on several factors including thermal conductivity through the PCB, electrical and thermal insulation layers, heatsink design, and the mechanical and thermal characteristics of the overall housing, etc.

CeraLink Capacitors

Polarization

In contrast to other ceramic capacitors, CeraLink capacitors are supplied with a defined polarity, as indicated on the case (with the exception of CeraLink 2220) and specified in the data sheet. This chapter explains the reasons for defining a polarity and describes its correct use in the application. The intention is to give the user a clear understanding of the relevant considerations for proper operation. Furthermore, we emphasize again that operation under continuous polarity change (AC) is not recommended, as it leads to significantly higher losses.

Note that the polarity marking is used primarily for incoming inspection, as the components are typically unpoled after reflow soldering due to thermal effects. When operated under normal DC-link conditions, i.e., at voltage levels $\geq V_{op}$, the polarization is re-established automatically within the first few seconds after the DC-link voltage is applied. However, when the components are operated below the specified operational voltage V_{op}, an initial polarization is required to achieve the full capacitance. The corresponding procedure, along with additional background information, is described in the following section.

Due to its specific material characteristics, CeraLink may be in a poled, unpoled, or reversely poled state, or in any intermediate condition. The polarization state can be reduced, eliminated or reversed through the application of voltage and/or temperature over time. In essence, there are three mechanisms to change or remove the polarization of CeraLink: voltage, time, and temperature.

Voltage

Applying a voltage polarizes the CeraLink in the direction of the applied voltage. When the voltage is sufficiently high, the polarization state becomes fully developed. An unpoled CeraLink typically exhibits only around 60% of its initial capacitance. This is commonly the case after thermal processes such as reflow soldering. As shown in Figure 22, the voltage required to fully polarize a CeraLink lies in the range of 90% to 95% of the rated voltage V_R. Note that under normal operating conditions, using the operational voltage V_{op}, the full polarization is generally not achieved, since $V_{op} < V_R$. This effect is particularly pronounced for the 500 V types, where V_{op} is 400 V – corresponding to only 80% of the rated voltage. For the 700 V and 900 V types, the corresponding ratios are approximately 86% and 89%, respectively.

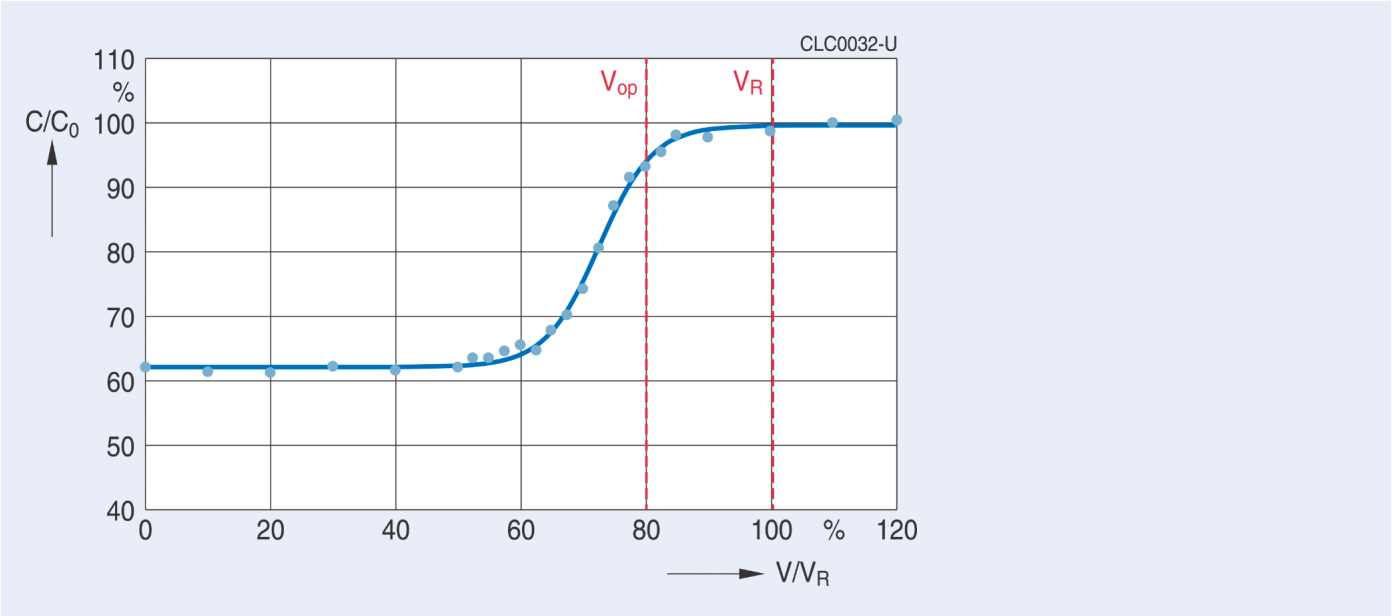


Figure 22: Required voltage to re-polarize a CeraLink capacitor.

Polarization

Voltage

It is important to note that polarization can fully reverse its direction when a sufficiently negative bias is applied. In this case, the polarization state changes and does not depend on time. The only requirement is that the full negative voltage is applied to the capacitor. The measured capacitance in both the polarized and reverse-polarized states is shown in Figure 23. The difference in capacitance becomes apparent only in the vicinity of the operating voltage. For small electric field strengths, no capacitance difference is observed. However, near the rated voltage, the device becomes effectively polarized during the measurement, causing the two curves to converge toward similar endpoints. When the voltage returns to 0 V, the curve corresponding to the originally “correctly polarized” state is reached again but mirrored in the opposite direction.

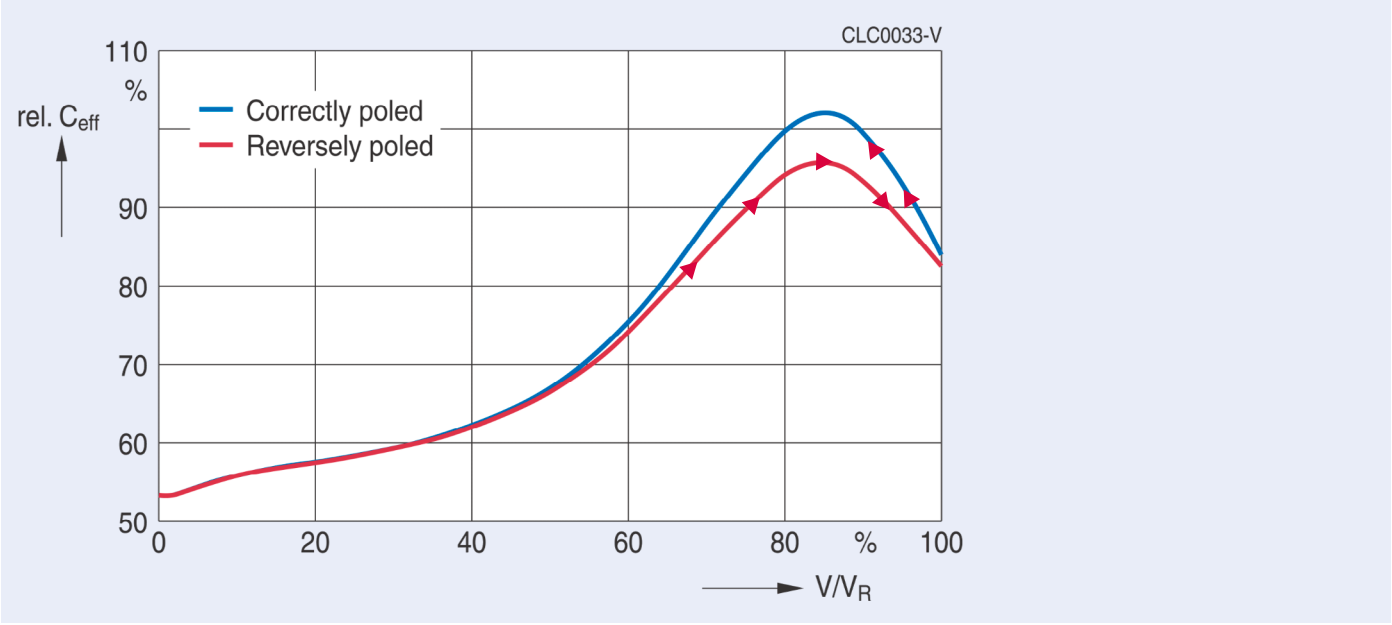


Figure 23: Measured capacitance in poling and in reverse poling direction.

Depolarization over time

CeraLink capacitors gradually lose polarization over time when no voltage is applied. At room temperature, the typical aging rate is approximately 2 to 2.5% per logarithmic decade. In practical terms, if the initial capacitance C_0 is measured one hour after polarization, it will decrease to roughly 98% after 10 hours, and 96% after 100 hours. This behavior is illustrated in Figure 24, which shows the measured data together with a fitted curve and the theoretical trend, assuming a 2.1% decrease per logarithmic decade.

Polarization

Depolarization over time

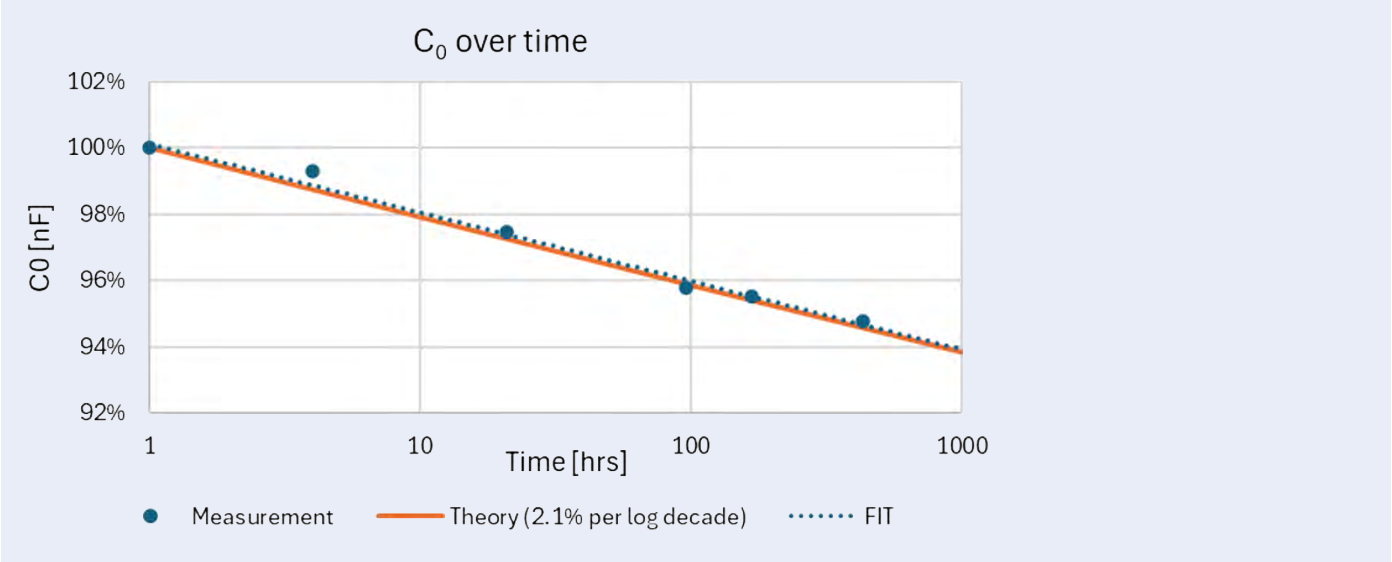


Figure 24: Comparison of the aging behavior of the initial capacitance (C_0): measured and fitted as well as the theoretical curve.

Please note that applying voltage to a component that has undergone aging can partially restore the initial capacitance C_0, but it will not recover to 100% of its original state. Full restoration is only possible by heating the component above its Curie temperature, as occurs during reflow soldering. However, since reflow soldering is typically part of the standard assembly process, this limitation is largely theoretical. It becomes relevant primarily during incoming inspection, for example when C_0 is measured at the customer site after extended storage.

Additionally, it is important to emphasize that the effective capacitance C_{eff}, which is usually the key parameter for practical applications, does not exhibit any significant aging over time. As shown in Figure 25, the time dependence of C_{eff} remains within the bounds of measurement uncertainty and is essentially flat.

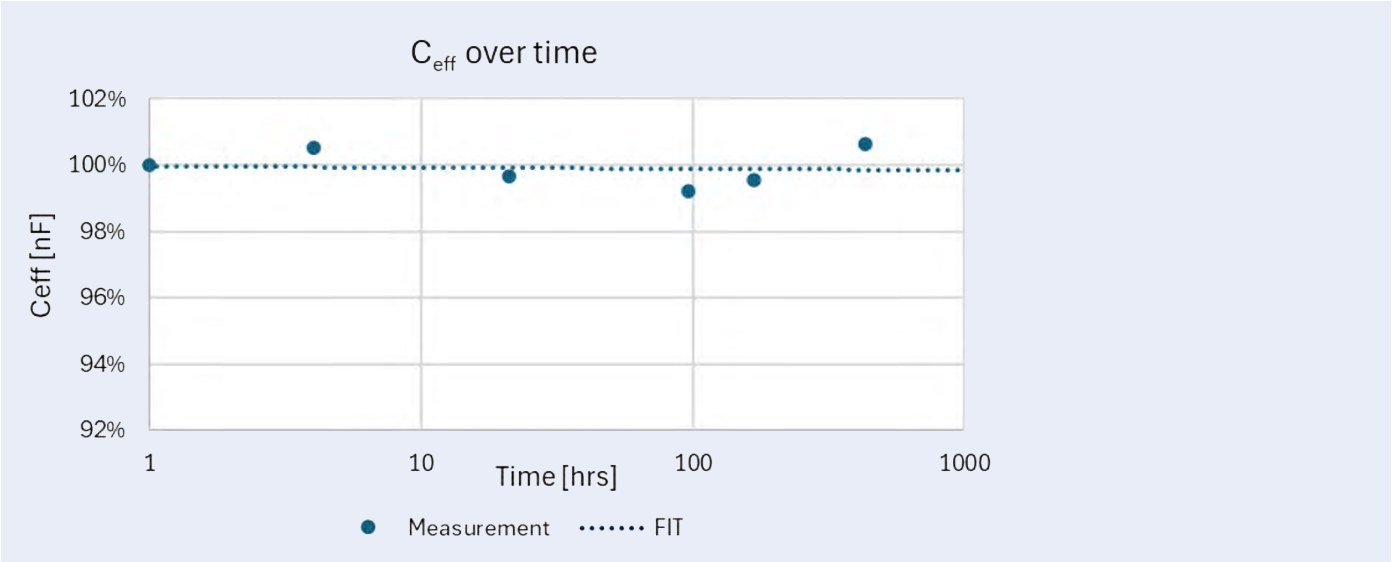


Figure 25: The effective capacitance C_{eff}, relevant for most applications, shows no measurable aging over time.

Polarization

Depolarization over time

The aging behavior of C_0 and its relationship to C_{eff} is shown in Figure 26 using a schematic representation. After passing the 100% end-of-line electrical test in our factory, the components gradually lose capacitance during storage, as previously described. This behavior is illustrated on the left-hand side by the solid blue Gaussian curve, representing a normally distributed production lot, and the dashed light-blue Gaussian curve, showing the same lot after a period of storage.

Although the C_0 distribution shifts over time as a result of aging, both the initial and aged distributions yield the same C_{eff} distribution within the expected measurement tolerance, as shown on the right-hand side.

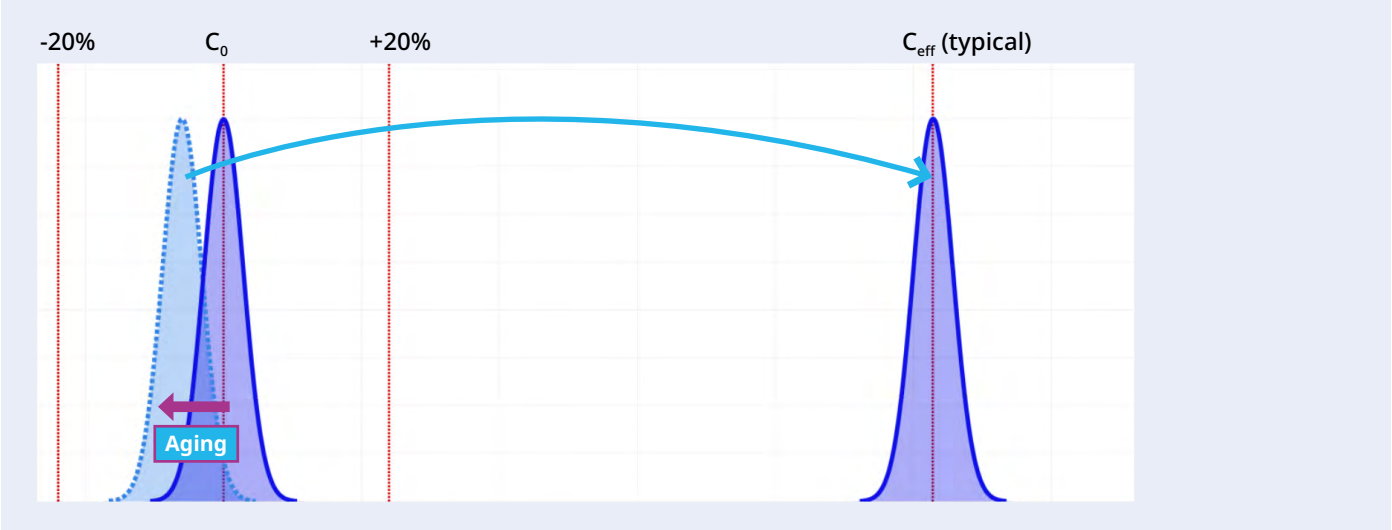


Figure 26: Schematic illustration of the aging behavior of C_0 and its relation to C_{eff}. The solid blue Gaussian curve on the right-hand side represents a production lot immediately after end-of-line testing at the factory, while the dashed light-blue curve shows the same lot after storage-induced aging. Despite the shift in C_0, both distributions result in the same C_{eff} distribution within measurement tolerance.

We emphasize that there is a strong and consistent correlation between C_0 and C_{eff}. Importantly, this relationship remains stable over time and is not influenced by aging effects, as illustrated in Figure 27.

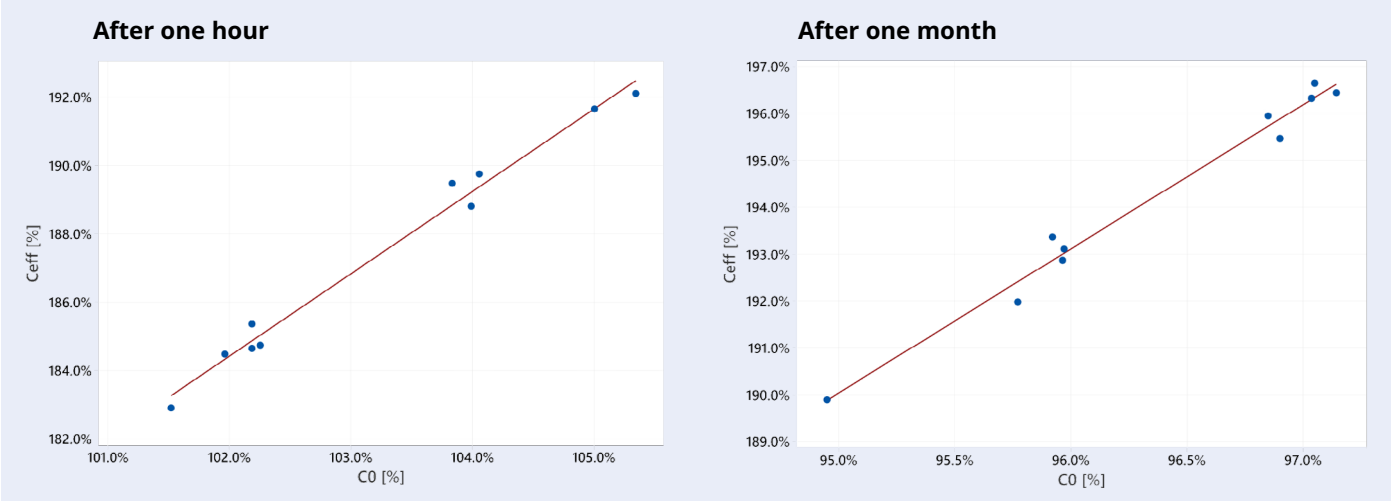


Figure 27: Strong correlation between C_0 and C_{eff}, which remains stable over time and is unaffected by aging.

Polarization

Depolarization over time

Figure 28 visualizes the correlation between C_0 and C_{eff} from a more practical perspective. Components with lower initial capacitance values (orange Gaussian) tend to exhibit lower effective capacitance, whereas those with higher initial values (green Gaussian) show correspondingly higher C_{eff}. Importantly, this relationship remains constant over time and is not affected by aging.

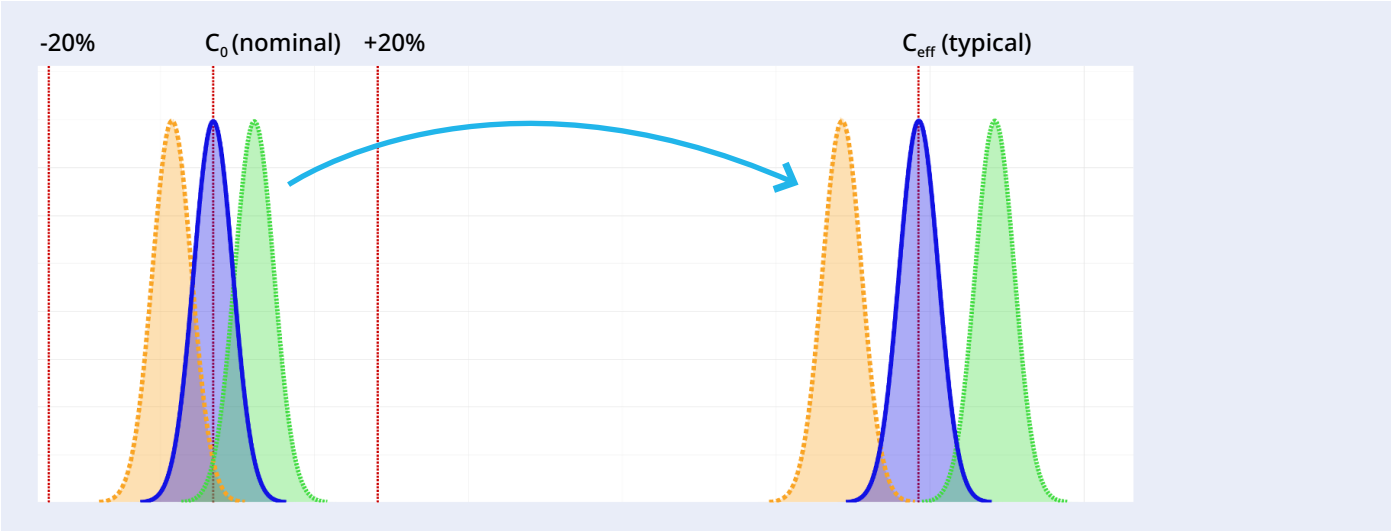


Figure 28: Correlation between C_0 and C_{eff} across different capacitance ranges. This correlation is not affected by aging.

Depolarization over temperature

The depolarization effect described above can be significantly accelerated when the component is exposed to elevated temperatures. In practical applications, this typically occurs during reflow soldering, where the component experiences temperatures exceeding its critical temperature T_c. Under these conditions, the material transitions into the paraelectric phase, as outlined in a previous section. Standard reflow soldering profiles – with peak temperatures of approximately +240 °C to +260 °C and exposure durations of several minutes – may result in partial depolarization of the CeraLink capacitor. This effect can be fully reversed by applying the rated voltage V_R (see section >Voltage<).

Polarization

Overview

Measuring the small-signal capacitance C_0 only provides the difference between the polarized and unpolarized states. Since the measurement itself has no inherent direction, the direction of polarization cannot be determined. When the rated voltage is applied, the device under test automatically polarized in the defined direction. Figure 29 schematically highlights the properties described above.

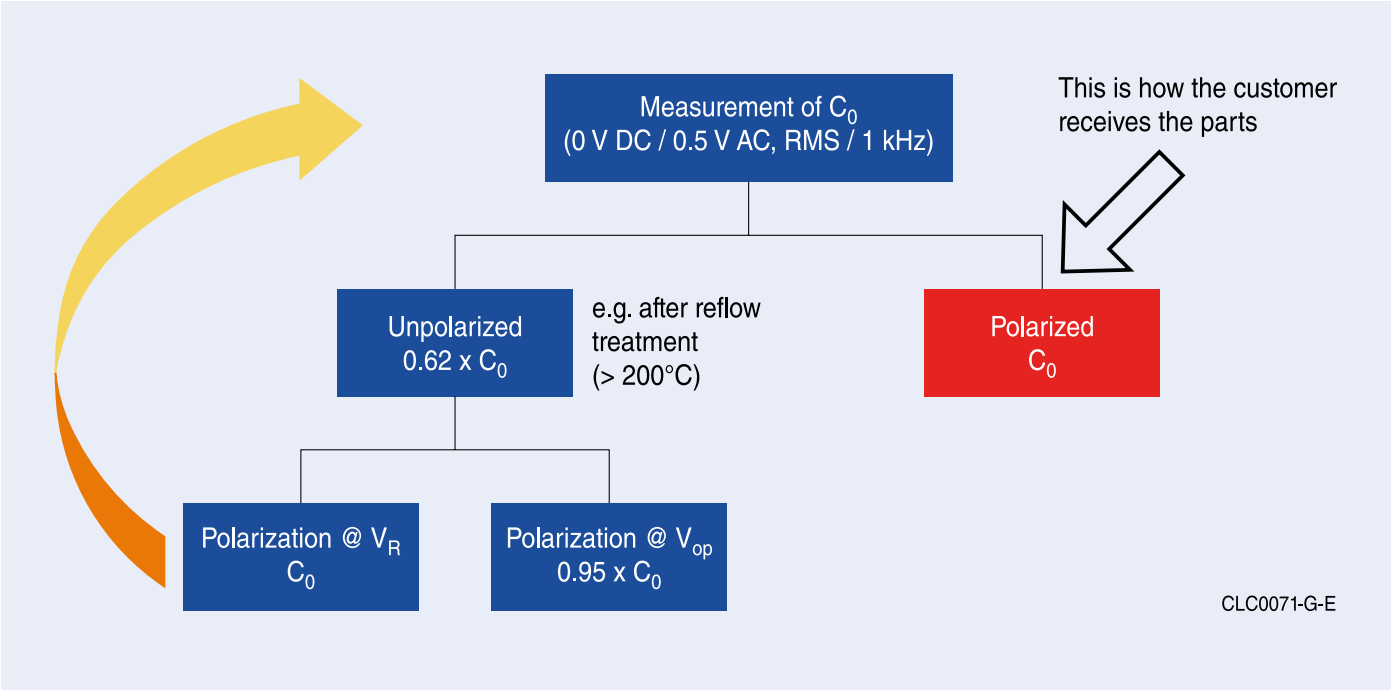


Figure 29: Schematic description of the relation between polarized state and capacitance value for CeraLink

CeraLink Capacitors

Lifetime model & lifetime estimation

The lifetime of a CeraLink depends on the applied voltage and the device temperature in the application. The corresponding acceleration parameters are determined through a Highly Accelerated Life Test (HALT). The lifetime under specific operating conditions can be evaluated by comparing the Weibull-distributed end-of-life measurements obtained at different voltages and temperatures, using the following Arrhenius-based model:

$$t_{char,app} = t_{char,ref}\left(\frac{U_{ref}}{U_{app}}\right)^{n} \times \exp\left[\frac{E_a}{k_b}\left(\frac{1}{T_{app}} - \frac{1}{T_{ref}}\right)\right]$$

k_b … Boltzmann constant (8,617 333 262 x 10^{-5} eV/K)

Model inputs	Parameters		500 V Type	700 V Type	900 V Type
Model parameters	n	voltage exponent		3.8	
	E_a	activation energy (in eV)		1.2	
Reference conditions*	U_{ref}	reference voltage level (in Volt)	600 V (150% V_{op})	900 V (150% V_{op})	1200 V (150% V_{op})
	T_{ref}	reference temperature (in Kelvin)		473.15K (200 °C)	
	$t_{char,ref}$	characteristic lifetime under reference conditions (in hours)		580 hours	
Application conditions	U_{app}	device voltage level in application (in Volt)		User input	
	T_{app}	device temperature in application (in Kelvin)			

*Note that the stated reference conditions might be different from our in-house testing conditions. The stated reference characteristic lifetime is valid for reference condition +200 °C and 150% V_{op}. Conversion between different conditions can be done via the above Arrhenius formula. The model parameters (e.g., activation energy) are based on experimental data and might be updated periodically.

Model output	Parameters	
	$t_{char,app}$	characteristic lifetime under application conditions (in hours)

Characteristic lifetime, reliability, and failure distribution

According to the Arrhenius law stated above, the characteristic lifetime $t_{char,app}$ can be determined for a given applied device voltage U_{app} and operating device temperature T_{app} in the application.

Once the characteristic lifetime has been determined, the corresponding reliability function is described by a Weibull distribution of the form:

$$R(t) = exp\left[-\left(\frac{t}{\tau_{char,app}}\right)^{\beta}\right]$$

R(t) represents the probability that the component remains functional "alive" at time *t*. The parameter β defines the slope of the Weibull distribution and is obtained from the HALT measurements. For CeraLink, this parameter is typically fixed at β = 2.5.

Lifetime model & lifetime estimation

Characteristic lifetime, reliability, and failure distribution

Note that since $\beta \neq 1$, the failure rate λ, which is related to the derivative of *R(t)*, obtains the more general formula:

$$\lambda(t) \equiv -\frac{1}{R(t)}\frac{dR(t)}{dt} = \frac{\beta}{\tau_{char,app}}\left(\frac{t}{\tau_{char,app}}\right)^{\beta-1}$$

Consequently, the failure rate is time-dependent, i.e. it varies with the operating time *t* of the system. This makes it less useful for practical lifetime assessment.

Therefore, it is often more convenient to consider the cumulative failure distribution function *F(t)* defined by:

$$F(t) \equiv 1 - R(t)$$

F(t) represents the cumulative failure amount, i.e., the probability that the component has failed by time t. By inverting this function, the specific lifetime *t* corresponding to a pre-defined cumulative failure amount (e.g., 0.1% or 100 ppm) can be determined using:

$$t(F) = \tau_{char,app} \times ln\left(\frac{1}{1-\mathrm{F}}\right)^{\beta^{-1}}$$

Note that the commonly used mean time to failure (MTTF) must be expressed using the more general form:

$$MTTF = \tau_{char,app} \times \Gamma\left[1+\frac{1}{\beta}\right]$$

Whereas the gamma function simplifies to Γ[2] = 1 for β = 1.

How to apply these formulas is exemplified in the following >Calculation Example I< .

CeraLink Capacitors

Lifetime model & lifetime estimation

Systems of identical chips

The extension to a system comprising multiple identical chips is straightforward. Let us consider the following series system of N identical components:

In this configuration, the entire system fails if any individual component fails. For example, a parallel arrangement of ceramic capacitors effectively behaves as a series system from a reliability standpoint, because a single capacitor short-circuit will cause the entire capacitor module or array to short.

The resulting reliability function for a system consisting of N identical components is given by:

$$R_{system}(t) = \prod_{i=1}^{N} exp\left[-\left(\frac{t}{\tau_{app,char}}\right)^{\beta}\right] = exp\left[-\mathrm{N}\left(\frac{t}{\tau_{app,char}}\right)^{\beta}\right] = exp\left[-\left(\frac{t}{\tilde{\tau}_{app,char}}\right)^{\beta}\right]$$

To bring the equation to equal form, we introduce the rescaled characteristic lifetime:

$$\tilde{\tau}_{app,char} \equiv \frac{\tau_{app,char}}{\sqrt[\beta]{N}}$$

Similar as in the previous case, the failure rate and MTTF is given by:

$$\lambda_{system}(t) = \lambda_1(t) + \lambda_2(t) + \cdots + \lambda_N(t) = \frac{\beta}{\tilde{\tau}_{char,app}}\left(\frac{t}{\tilde{\tau}_{char,app}}\right)^{\beta-1}$$

$$MTTF_{system} = \tilde{\tau}_{char,app} \times \Gamma\left[1 + \frac{1}{\beta}\right]$$

Lifetime model & lifetime estimation

Mission profiles and combined failure distributions

In real-world applications, the operating conditions (device temperature and applied voltage) are typically not constant but fluctuate significantly over the lifetime of the device. To some extent, this complex behavior can be approximated by a mission profile that groups the continuous ups and downs of temperature and voltage into several subsequent constant regions (see Figure 30 for an example).

The extension of the previous approach to multiple consecutive operating conditions is straightforward. The resulting reliability function is obtained as the product of the individual reliability functions and is therefore given by:

$$R_{total}(t_1; \dots; t_N) = \prod_{i=1}^{N} R_i(t_i) = \prod_{i=1}^{N} exp\left[-\left(\frac{t_i}{\tau_{app,char}^{(i)}}\right)^{\beta}\right]$$

With the individual characteristic lifetimes $\tau_{app,char}^{(i)}$ and operating times t_i the system is operated under a specific application condition "*i*" (i.e. a specific device temperature and voltage).

Analogously, the cumulative failure distribution function is defined by:

$$F_{total}(t_1; \dots; t_N) \equiv 1 - R_{total}(t_1; \dots; t_N)$$

This generalized approach is exemplified in the following Calculation Example II – Simplified Mission Profile.

Finally, when considering the mission profile approach for a system of identical chips, the total reliability function is given by:

$$R_{total}(t_1; \dots; t_N) = \prod_{i=1}^{N} exp\left[-M\left(\frac{t_i}{\tau_{app,char}^{(i)}}\right)^{\beta}\right] = \prod_{i=1}^{N} exp\left[-\left(\frac{t_i}{\tilde{\tau}_{app,char}^{(i)}}\right)^{\beta}\right]$$

Where, analogously to the previous section, we introduced the re-scaled characteristic lifetime: "M" is the number of identical chips.

$$\tilde{\tau}_{app,char}^{(i)} \equiv \frac{\tau_{app,char}^{(i)}}{\sqrt[\beta]{M}}, \qquad with\ i \in [1, \dots, N]$$

Lifetime model & lifetime estimation

Calculation example I – constant operating conditions

In this example, we consider the CeraLink LP 500 V type. Three different operating temperatures and two different voltage levels are evaluated over the lifetime of the component.

Please note that, for lifetime calculation, the decisive factors are the operating temperature and voltage experienced by the chip. Whether the chip reaches its operating temperature due to self-heating from electrical current or due to elevated ambient temperature is irrelevant.

Table 3 shows the characteristic lifetime in hours, as well as the lifetime for 1% and 10 ppm failure amounts, and the MTTF. Note that due to the underlying Weibull–type distribution, 63.2% of the samples will have statistically failed after the characteristic lifetime.

Please note that this example calculation provides only a rough estimation. A detailed lifetime assessment requires a dedicated mission profile (see also the following example).

U_{op} \ T_{op}	100 °C	125 °C	150 °C
400 V	$\tau_{char,app} = 7.21 \times 10^6$	$\tau_{char,app} = 6.92 \times 10^5$	$\tau_{char,app} = 87700$
	$\mathrm{MTTF} = 6.40 \times 10^6$	$\mathrm{MTTF} = 6.14 \times 10^5$	$\mathrm{MTTF} = 7.78 \times 10^4$
	$t_{1\%} = 1.15 \times 10^6$	$t_{1\%} = 1.10 \times 10^5$	$t_{1\%} = 13900$
	$t_{10ppm} = 72100$	$t_{10ppm} = 6920$	$t_{10ppm} = 877$
500 V	$\tau_{char,app} = 3.09 \times 10^6$	$\tau_{char,app} = 2.97 \times 10^5$	$\tau_{char,app} = 37600$
	$\mathrm{MTTF} = 2.74 \times 10^6$	$\mathrm{MTTF} = 2.63 \times 10^5$	$\mathrm{MTTF} = 3.33 \times 10^4$
	$t_{1\%} = 4.90 \times 10^5$	$t_{1\%} = 47100$	$t_{1\%} = 5960$
	$t_{10ppm} = 30900$	$t_{10ppm} = 2970$	$t_{10ppm} = 376$

Table 3: Lifetime calculation for CeraLink LP 500 V. All shown lifetimes in hours.

TDK points out that the experimental test boundary condition for no failure is the High Temperature Operational Life test (MIL-STD-202, method 108) at rated voltage and +150 °C for 1000 hours.

Nevertheless, due to the statistical nature of the failure mechanism, a zero-failure rate within this time cannot be guaranteed.

CeraLink lifetime model & lifetime estimation

Calculation example II – simplified mission profile

We consider the following mission profile for a CeraLink LP 900 V type, with three discrete operating conditions: 750 V DC / +85 °C, 800 V DC / +115 °C and 850 V DC / +135 °C

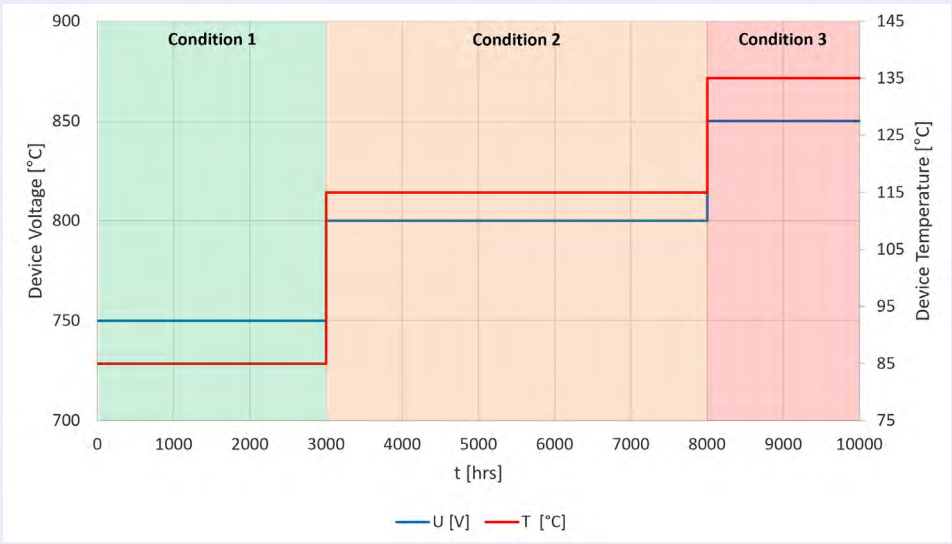


Figure 30: Simple mission profile

The contributions of the individual conditions are given by:

Condition 1: Characteristic lifetime: $\tau_1 = 4.42 \times 10^7$ h
The cumulative failure amount is given by (using $t_1 = 3000$ h):

$$F_1(t_1) = 1 - exp\left[-\left(\frac{t_1}{\tau_1}\right)^{\beta}\right] = 3.80 \times 10^{-11} = 0.038\ ppb$$

Condition 2: Characteristic lifetime: $\tau_2 = 1.71 \times 10^6$ h
The cumulative failure amount is given by (using $t_2 = 5000$ h):

$$F_2(t_2) = 1 - exp\left[-\left(\frac{t_2}{\tau_2}\right)^{\beta}\right] = 4.62 \times 10^{-7} = 0.462\ ppm$$

Condition 3: Characteristic lifetime: $\tau_3 = 2.34 \times 10^5$ h
The cumulative failure amount is given by (using $t_3 = 2000$ h):

$$F_3(t_3) = 1 - exp\left[-\left(\frac{t_3}{\tau_3}\right)^{\beta}\right] = 6.67 \times 10^{-6} = 6.67\ ppm$$

The combined contributions, i.e., the total cumulative failure amount after 10,000 hours, are given by:

$$F_{total}(t_1; t_2; t_3) = 1 - exp\left[-\left(\frac{t_1}{\tau_1}\right)^{\beta}\right] exp\left[-\left(\frac{t_2}{\tau_2}\right)^{\beta}\right] exp\left[-\left(\frac{t_3}{\tau_3}\right)^{\beta}\right] = 7.22 \times 10^{-6} = 7.22\ ppm$$

CeraLink Capacitors

Handling of CeraLink - General remarks

General guidelines applicable to all CeraLink products are summarized below. Depending on the specific product selected, additional instructions may be provided in the corresponding data sheet.

General handling instructions for CeraLink components

- Avoid mechanical damage: Do not drop CeraLink components or allow them to be chipped.
- Use protective equipment: Avoid direct contact with bare hands. Use gloves.
- Prevent contamination: Ensure that the surface of the CeraLink component remains clean during handling.
- Proper pick-and-place handling: Do not clamp components on their face sides. A vacuum-based pick-and-place process that grips the component from the top side is recommended.
- Cautious cleaning: Washing processes (e.g., to remove flux residues) may be used but should be applied with care. Static or cyclic mechanical stress – such as that from ultrasonic cleaning – can damage the product. Any mechanical stress that could cause cracks must be avoided to preserve reliability and lifetime.
- Mechanical stress considerations: CeraLink LP (Low Profile) and FA (Flex Assembly) series use copper-invar-copper (CIC) lead frames to minimize stress on the ceramic. Excessive bending or twisting – especially after soldering – can lead to detachment of the lead frame and should be avoided.

General mounting instructions for CeraLink components

- Encapsulation caution: Encapsulating CeraLink devices with sealing or overmolding materials may degrade electrical performance and reduce product lifetime. Mechanical stress during these processes should be avoided, and heat dissipation capability may be negatively affected. Please contact TDK for further guidance.
- Adhesive use: Board fixation using SMD adhesives is generally discouraged. Adhesives with high Shore hardness and mismatched coefficients of thermal expansion (CTE) can induce mechanical stress and cause ceramic cracking. If fixation is necessary, use adhesives with low Shore hardness and CTE $\leq$10 ppm/K.
- Electrode protection: Do not scratch the electrodes at any stage of the mounting process.
- Component integrity: Ensure the CeraLink component is not damaged before, during, or after mounting (e.g., during pick-and-place).
- Clean assembly: Contacts and housings used in conjunction with CeraLink components must be clean before mounting.
- Thermal spacing: During operation, the surface temperature of CeraLink components may exceed ambient temperature. Maintain adequate spacing to adjacent components to ensure proper cooling.
- Surface cleanliness: Avoid contamination of the CeraLink surface throughout the processing steps.

CeraLink Capacitors

CeraLink lead frame connection

The lead frames are connected via silver sintering to the ceramic body, as shown in the following schematic and microscope pictures.

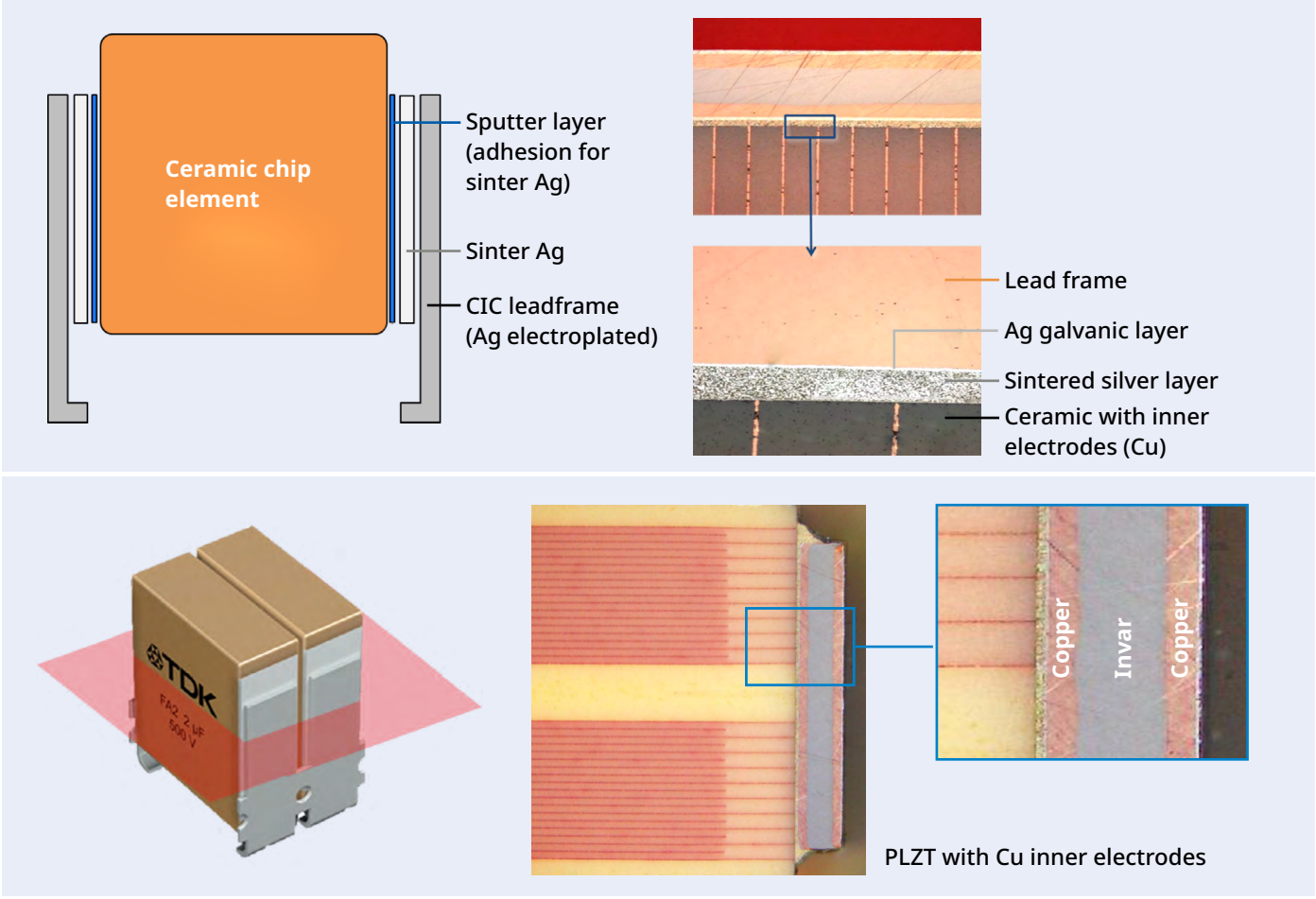
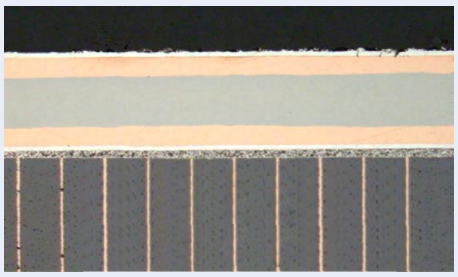


Figure 31

The sintered silver connection offers several advantages, particularly in terms of thermal management and compatibility with the ceramic's coefficient of thermal expansion (CTE). Due to the high homologous temperature of silver compared to solder, it exhibits excellent stability under rapid temperature changes – as demonstrated in Figure 32:



No crack or damage after 10 k thermal cycles (–55 °C to +155 °C)

Figure 32

In general, all materials used in the connection provide outstanding thermal and electrical conductivity, resulting in very low thermal resistance. However, from a mechanical perspective, sintered silver connections require more careful handling than soldered joints, as outlined in the following section.

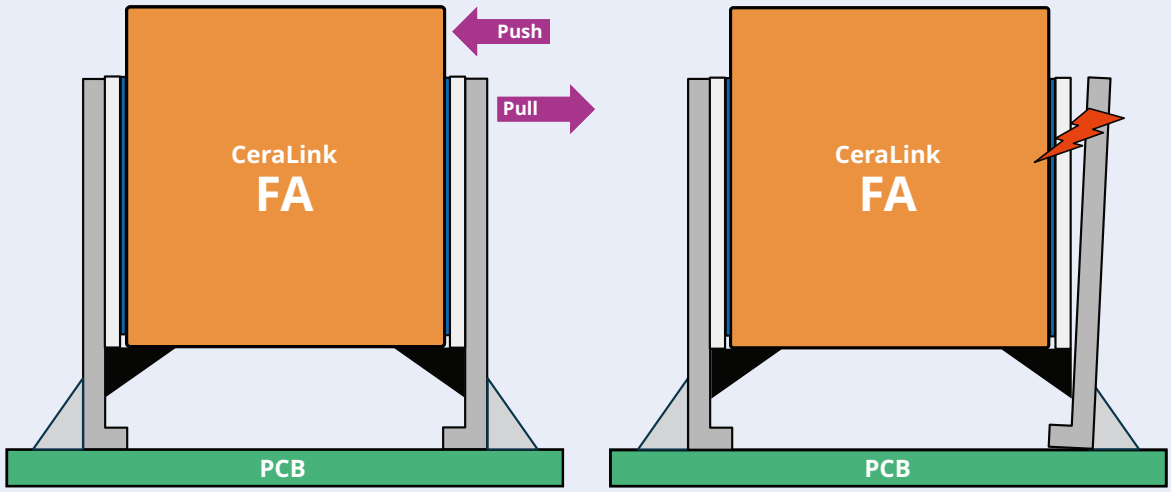
CeraLink Capacitors

CeraLink lead frame connection

Excessive external mechanical force

Excessive mechanical force applied to either the lead frame or the ceramic chip element can compromise the sintered silver connection, potentially leading to detachment of the lead frame. From a technical standpoint, a detached lead frame poses a serious risk: although it may appear electrically open, applying voltage can result in flashovers between the lead frame and the ceramic body. Such flashovers can progressively damage the ceramic chip element, ultimately causing a short circuit of the entire component.

Flex Assembly (FA) series:



Low Profile (LP) series (example of J-style type)**:**

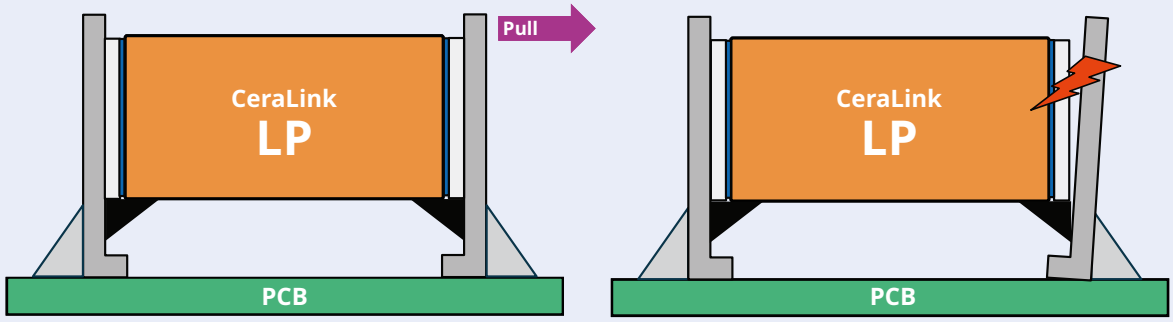


Figure 33

CeraLink lead frame connection

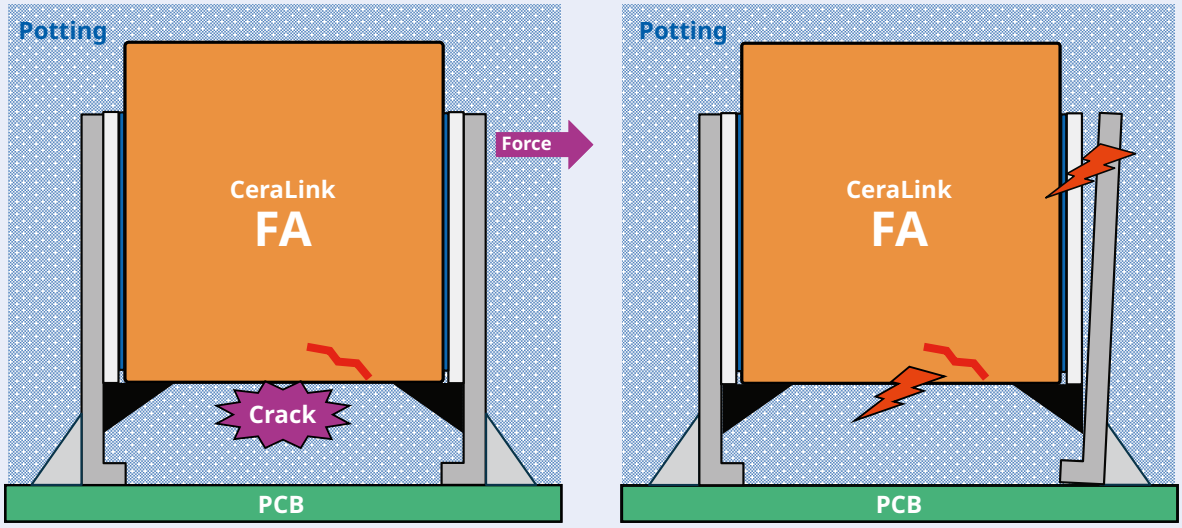
Potting or fixation with unsuitable materials

Certain potting materials – particularly hard, epoxy-based types – can impose significant (thermo-mechanical stress on the ceramic chip element and the lead-frame connection. Such stress may occur during the curing process or later in operation due to mismatched CTEs. These effects can lead to cracks in the ceramic, damage to the sintered-silver connection, or, in severe cases, detachment of the lead frame.

Similarly, SMD adhesives should generally be avoided for board fixation of CeraLink components. Adhesives with high Shore hardness or with a CTE significantly different from that of the component can induce mechanical stress and lead to ceramic cracking. If mechanical fixation is unavoidable, adhesives with low shore hardness and a CTE ≤10 ppm/K are recommended.

In all cases, the chemical and mechanical compatibility of potting materials or adhesives must be carefully evaluated for the specific application.

Flex Assembly (FA) series:



Low Profile (LP) series (example of J-style type)**:**

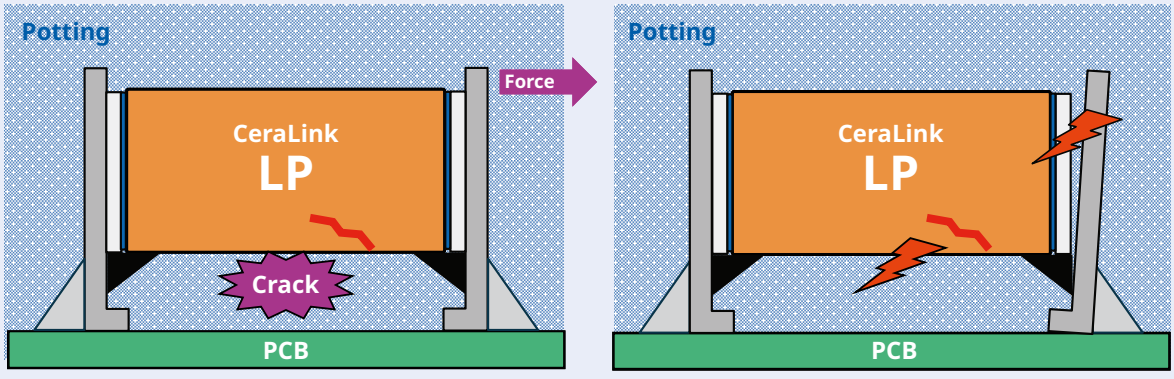


Figure 34: Schematic description of potential problems induced by potting

CeraLink lead frame connection

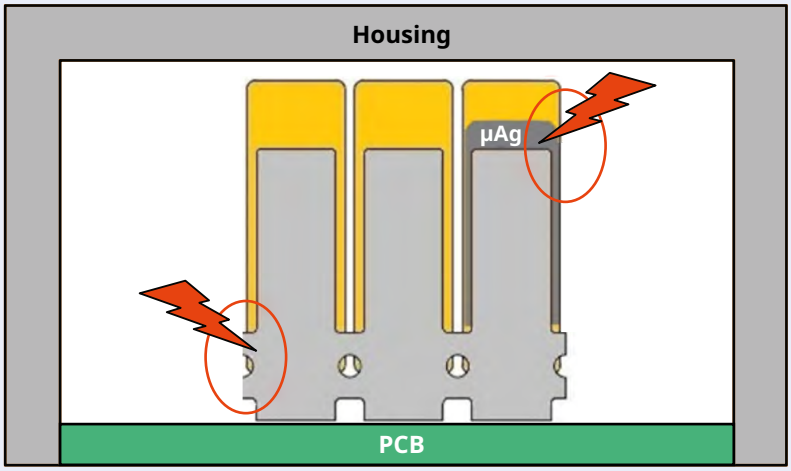
Insufficient clearance distance

Insufficient clearance distances can lead to electrical flashovers to the housing or other exposed parts of the PCB, such as screw terminals. These flashovers may cause localized damage to the lead frame or ceramic chip element and can ultimately result in short circuits. Additionally, depending on the expected level of contamination in the application environment, a conformal coating may be required to meet regulatory creepage distance requirements.

In case of any uncertainty regarding potential chemical incompatibility, please contact TDK for further guidance.

Further information on creepage and clearance distance is available in the FAQ section of this document and in the data sheets.

Flex Assembly (FA) series:



Low Profile (LP) series (example of J-style type)**:**

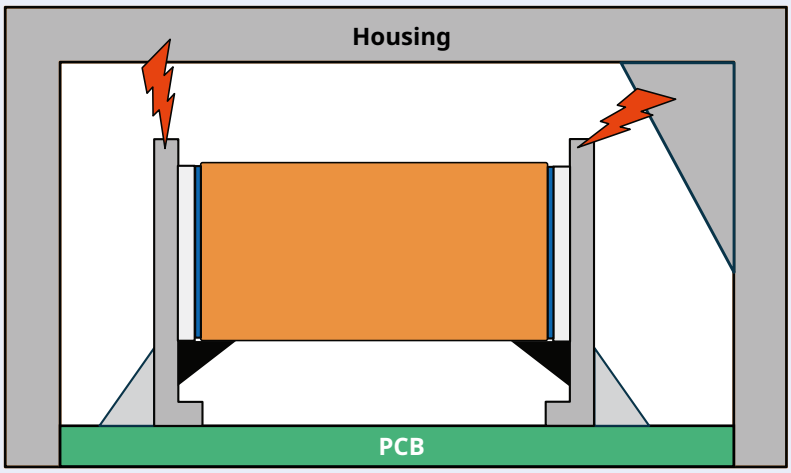


Figure 35

CeraLink Capacitors

Frequently asked questions (FAQs)

How do I detect if CeraLink is polarized or unpolarized?

Measure the small signal capacitance C_0 as described in the data sheet (typically at 0 V, 0.5 V AC, 1 kHz). If the measured value C_0 is only about 60% of the data sheet specification, the CeraLink capacitor is unpolarized (which is typically the case after reflow soldering).

CeraLink seems to be partly polarized/unpolarized (e.g., after reflow soldering). How shall I proceed?

During operation – i.e., when DC bias voltage $\geq V_{op}$ is applied – the CeraLink capacitor becomes polarized. If a fully polarized component is required prior to operation, the rated voltage V_R should be applied to the device. This is particularly important in applications where the capacitor is not continuously biased, such as in protection circuits.

In such cases, applying a defined voltage profile after reflow soldering is recommended to ensure that the device is fully polarized in the event of a fault (voltage pre-conditioning).

If CeraLink is polarized, how do I detect the polarizing direction?

The only practical method to detect the polarization direction of a CeraLink is to measure the effective capacitance C_{eff}, i.e., to perform the C_0 measurement under DC bias (noting that C_{eff} is defined as C_0 at the operating voltage V_{op}). In this measurement, a slightly lower capacitance value will be observed if the CeraLink is polarized in the reverse direction (Figure 23). This effect is most pronounced for the 500 V type and becomes less distinct for higher-voltage classes (see previous discussion). In general, the simpler and more robust approach is to reset the polarization by applying the rated voltage V_R.

What happens if a CeraLink capacitor is mounted in the wrong polarization direction?

a) If V_R is applied, the capacitor becomes fully re-polarized during the first switching on. No further action is required.

b) If V_{op} is applied in the application, two scenarios should be considered:

1. V_{op} with a small, superimposed ripple voltage (small-signal condition): The capacitor will polarize to a level of ≥95%, corresponding to a capacitance reduction of ≤5%.

2. V_{op} with a large, superimposed ripple voltage (large-signal condition): The additional ripple amplitude is generally sufficient to fully polarize the CeraLink.

c) If a voltage lower than V_{op} is applied in the application, it is recommended to mount the CeraLink capacitor with a pre-defined polarity. Note that after reflow soldering and/or time exposure, the CeraLink may be partly unpolarized (see chapter >Polarization<).

Frequently asked questions (FAQs)

Where can I see polarity?

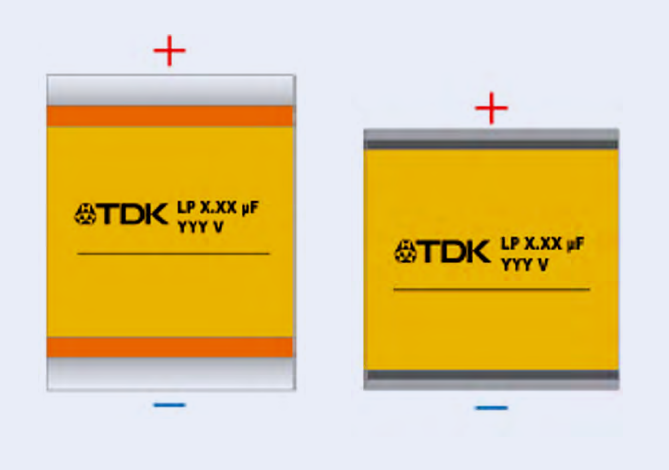


Figure 36: Polarity of CeraLink LP.

The polarity is described in the respective data sheet, located after the dimensional drawing and the solder-pad recommendations. As an example, Figure 36 illustrates the polarity for the CeraLink LP version. Note that this is intended solely for incoming inspection, and has no impact on device operation. When subjected to reverse rated voltage V_R, the CeraLink becomes repolarized and continues to operate identically. Furthermore, CeraLink 2220 components do not include any polarity for this reason.

No limitation on dv/dt is specified. How should this be interpreted with respect to voltage or current peaks occurring in the millisecond range?

The dV/dt ratio is limited solely by the intrinsic ESR of the CeraLink, where the time constant τ is defined as $\tau = ESR \cdot C$. Since the ESR is nonlinear and depends on both frequency and temperature, it is difficult to specify a universal value for τ. However, under typical application conditions, the time constant lies in the nanosecond range, i.e., well below the microsecond range.

Furthermore, please note that there is, in principle, no inherent limitation on the di/dt. In other words, short peak current pulses are fundamentally constrained only by two factors:

1. The overall induced voltage (e.g., arising from stray inductance or highly inductive loads) on the capacitor must remain below $V_{pk,max}$ and
2. The induced device temperature stays within the rated limits.

What do I have to consider regarding conformal coating?

Depending on the expected level of PCB contamination in the intended application, a conformal coating may be necessary to comply with normative creepage-distance specifications. In cases where potential chemical incompatibilities are uncertain, please contact TDK for further guidance.

In general, TDK does not recommend potting or encapsulation of CeraLink components with rigid, epoxy-based materials, as such materials can induce mechanical stress and potentially cause cracking in the ceramic. Soft, gel-type potting materials – commonly used in power-module integration – are typically more suitable. In all cases, when potting or encapsulation is being considered for a specific application, please consult TDK.

CeraLink Capacitors

Frequently asked questions (FAQs)

What do I have to consider regarding creepage and clearance distance?

CeraLink ceramic typically has a relatively large Comparative Tracking Index (CTI) of ≥ 600. Therefore, it fulfills the requirements on creepage and clearance distance according to IEC 60664-1 for degree of contamination 1 or 2 for all voltage types:

Degree of contamination			
CeraLink V classes	1	2	3
500 V (LP & FA)	Yes (> 1.3 mm)	Yes (> 2.5 mm)	Not recommended
700 V (LP & FA)	Yes (> 2.0 mm)	Yes (> 3.5 mm)	Not recommended
900 V (LP & FA)	Yes (> 3.2 mm)	Yes (> 4.5 mm)	Not recommended

Table 4: Creepage distance requirements according to IEC 60664-1 Table F.5 for contamination class 1 & 2 are fulfilled for all CeraLink LP & FA types.

Degree of contamination			
CeraLink V classes	1	2	3
500 V (2220)	Yes (> 1.3 mm)	Yes (> 2.5 mm)	Not recommended
900 V (2220)	Yes (> 3.2 mm)	No (> 4.5 mm)	Not recommended

Table 5: Note that the creepage distance requirement according to IEC 60664-1 Table F.5 for contamination class 2 is not fulfilled for the CeraLink 2220 900 V. Additional measures (e.g., conformal coating and/or slitting of PCB) are recommended for this type.

Which soldering processes are applicable for CeraLink?

CeraLink series	Reflow*	Wave	Other (e.g., vapor phase)
LP, FA	Recommended	Not recommended	Please consult TDK
SP (terminated)	Recommended	Recommended	Please consult TDK
2220	Recommended	Not recommended	Please consult TDK

Table 6: Soldering processes

How can I repair/rework soldering on CeraLink?

Manual soldering using a soldering iron should be avoided. If this is not possible, hot-air methods are recommended for repair.

* Reflow soldering profiles according to IEC 60068-2-58 recommendations. For details, please check the respective product data sheet. The usage of lead-free solder types is recommended.

CeraLink Capacitors

Frequently asked questions (FAQs)

Is CeraLink using the classical MLCC design?

The CeraLink ceramic chip features a multilayer serial connection (MLSC) design, i.e., a series connection of two MLCC geometries in one component, as shown in Figure 37. Compared to the standard MLCC design, this design offers additional safety and can reduce the risk of short circuits caused by ceramic cracks (e.g., resulting from mechanical overstress).
If one side of the MLSC is shorted, the other side can theoretically withstand the rated voltage V_R, though this will reduce the overall lifetime. Furthermore, MLSC minimizes the risk of surface arcing or other surface migration effects, such as Ag migration.

However, the MLSC design should be considered only as a safety feature and cannot prevent short circuits.

This is particularly true for high-power/high-voltage applications, where a short circuit on one side of the MLSC can affect the other side as well due to the significant amount of energy stored. Therefore, in principle, a ceramic crack in a CeraLink or overvoltage can lead to a short circuit, as with other ceramic capacitors. Additionally, the capacitance density of an MLSC is lower than that of a traditional MLCC design.

Note that the CeraLink 2220 series is designed for the highest capacitance density and therefore features the traditional MLCC design. In this case, the risk of ceramic cracking is reduced via an additional soft termination layer (for soft termination type only).

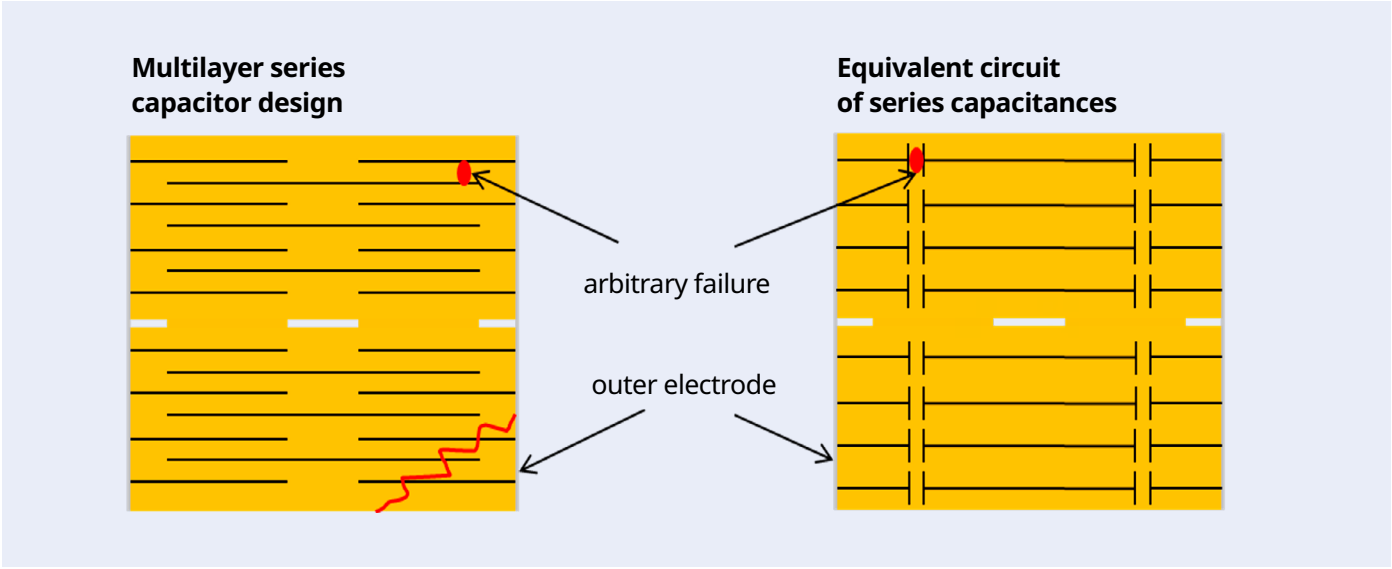


Figure 37: MLSC design of CeraLink standard chip (LP, FA & SP).

CeraLink Capacitors

Frequently asked questions (FAQs)

Why can CeraLink handle so much current?

CeraLink chips incorporate copper inner electrodes that provide excellent electrical conductivity and low losses, as well as outstanding thermal performance. Heat generated within the chip is efficiently transferred to the outer contacts (lead frames) and subsequently to the PCB.

The CeraLink ceramic body is connected to the outer contacts through a sintered silver layer. The outer contacts are made of CIC (copper-invar-copper), which offers the highest electrical and thermal conductivity while maintaining a low coefficient of thermal expansion (CTE). Additionally, the CTE is matched to that of the ceramic to minimize the thermo-mechanical stress within the whole system.

In conclusion, all materials used provide excellent thermal and electrical conductivity, ensuring efficient heat transfer from the component through the lead frames to the PCB. This is especially the case for CeraLink LP and FA series. However, an appropriate cooling concept is essential to support the required current-handling capability, as shown in the chapter >Current Capability<. Please note that all data sheet values are based upon worst-case conditions (mounting on standard FR4, without a heatsink, and without active airflow).

What about pulse current and inrush current?

The pulse-current capability of CeraLink is typically several orders of magnitude higher than the continuous (RMS) current capability specified in the data sheet. Pulse currents can reach several kA without damaging the device. However, it strongly depends on the application conditions if such a current pulse will induce a harmful voltage on the device (e.g., due to the overall inductance in the system).

Furthermore, very large current pulses may induce hot spots within the capacitor, which can lead to localized defects in the ceramic material. Conversely, a pulse that is not critical as a singular event may significantly heat the capacitor if applied repeatedly. In this case, the pulse currents must be considered because they contribute to self-heating.

Therefore, the pulse current capability is not usually stated in the data sheet and must be tested for each application. For questions regarding the pulse current capability of CeraLink for a particular application, please consult TDK.

Inrush current is a parameter that is more relevant and discussed in the context of other capacitor technologies, such as “metalized polypropylene film capacitors” or “aluminum electrolytic capacitors”. Ceramic capacitors are usually not subject to such restrictions.

CeraLink Capacitors

Frequently asked questions (FAQs)

How much lead (Pb) does CeraLink contain?

CeraLink ceramic contains approximately 60% by weight of lead (Pb) in covalent and ionic bonds.

Note that for CeraLink, the RoHS exemption 7(c)-II, lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher, is valid. Thus, CeraLink capacitors can be used without any further restrictions.

Further details on this topic, as well as on the material composition, are available in the material data sheet on our website: www.tdk-electronics.tdk.com

Which MSL does apply?

In general, CeraLink components are not moisture sensitive, and therefore, the Moisture Sensitivity Level (MSL) does not apply. If required, MSL = 1 can be used. Nevertheless, use CeraLink as soon as possible after opening factory seals such as polyvinyl-sealed packages, since solderability might degrade (particularly when exposed to a corrosive atmosphere).

Are balancing resistors needed when connecting CeraLinks in series?

Voltage imbalances can lead to an asymmetrical operation of capacitors in serial connection. In this case, one of the capacitors will operate at a lower voltage while the other one operates at a higher voltage (compared to the symmetric case). Under normal circumstances, a slight voltage imbalance is not critical. However, in some cases, balancing resistors may be necessary in some cases to compensate for this imbalance.

The voltage imbalance might be introduced by different device temperatures between the capacitors, leading to slightly different capacitance and ESR values. However, TDK notes that even though CeraLink shows a non-linear behavior over temperature and voltage, the temperature differences are usually not sufficient to lead to a significant imbalance. Additionally, the CeraLink ceramic has some self-regulating properties, so it is quite unlikely that the two capacitors in series will drift apart. Nevertheless, please consult TDK in case of doubt.

CeraLink Capacitors

Appendices

Glossary

Symbols	Terms
AC	Alternating current
AFE	Antiferroelectric
C_0	Initial capacitance at 0 V DC, 0.5 V AC (RMS), 1 kHz, room temperature
C_{eff} ($C_{eff, typ}$)	Typical effective capacitance at V_{op}, 0.5 V AC (RMS), 1 kHz, room temperature
C_{nom} ($C_{nom, typ}$)	Typical nominal capacitance at V_{op}, quasistatic, room temperature
CIC	Copper-invar-copper
CTE	Coefficient of thermal expansion
CTI	Comparative tracking index
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
FA	Flex assembly
FE	Ferroelectric
f_{ripple}	Frequency of the operation ripple current
I_{op}	Operating ripple current, root mean square value of sinusoidal AC
LP	Low profile
MLCC	Multilayer ceramic capacitor
MLSC	Multilayer serial capacitor
PCB	Printed circuit board
PE	Paraelectric
PLZT	Lead lanthanum zirconium titanate
ppm	Parts per million
R_{ins}	Insulation resistance at V_{pk}, measurement time 7 s, room temperature
SP	Solder pin (note that this component is terminated with 04/2024)
T_{amb}	Ambient temperature
T_C	Critical temperature
tan δ	Dissipation factor at 0 V, 0.5 V AC (RMS), 1 kHz, room temperature
T_{device}	Device temperature. $T_{device} = T_{amb} + \Delta T$ (ΔT defines the self-heating of the device due to applied current)
V_{op}	Operating voltage
V_R	Rated voltage
$V_{AC, RMS}$	Root mean square value of sinusoidal AC voltage
$V_{pk, max}$	Maximum peak operating voltage according CeraLink data sheet
ΔT	Increase of temperature during operation

CeraLink Capacitors

Appendices

CeraLink data sheet

Please find all our latest CeraLink data sheets on the TDK webpage here:
Product catalog: CeraLink capacitors | TDK Electronics - TDK Europe
CeraLink Capacitors | Products | TDK Product Center

Design support

TDK is continuously working on extending its library of design support tools.
On the TDK webpages, several possible use cases/functions are shown in application notes.

Contact information

For further information and support, please contact our team via the following email address:
ceralink@tdk.com

Revision history

Revsion	Changes
V3 (March 2026)	Physical background for capacitance behavior added; handling guide added, editorial changes
V2 (July 2024)	Marking of CeraLink SP series as terminated, update of lifetime estimation, new FAQ, editorial changes
V1 (Jan 2021)	Original

Important information
Some parts of this publication contain statements about the suitability of our products for certain areas of application. These statements are based on our knowledge of typical requirements that are often placed on our products. We expressly point out that these statements cannot be regarded as binding statements about the suitability of our products for a particular customer application. It is incumbent on the customer to check and decide whether a product is suitable for use in a particular application. This publication is only a brief product survey which may be changed from time to time. Our products are described in detail in our data sheets. The *Important notes* (www.tdk-electronics.tdk.com/ImportantNotes) and the product-specific *Cautions and warnings* must be observed. All relevant information is available through our sales offices.

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