Pressure Sensors

Reliability and long-term stability for pressure sensing dies

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Contents

1. Scope

The purpose of this document is to provide a guideline for advanced qualification of the reliability and long-term stability of pressure sensor dies with specific tests, based on TDK`s experience with pressure sensor dies, supplemented by customer experience in related application areas.

Following this approach, general failure mechanisms in related applications for dies were considered to determine a set of reliability tests capable of stimulating and triggering general pressure sensor die failures.

This document defines the parameters for characterizing the long-term stability of pressure sensor dies and the related tests which TDK uses as a standard specification for estimating these parameters.

2. General information

For the characterization of the long-term stability of pressure sensor dies, only the offset voltage parameter is used. The stability of a silicon pressure sensor die can be characterized by the stability of the offset voltage. Electronic surface effects (e. g. mobile ions in the silicon oxide), which affect the surface conductivity, only influence the offset voltage, but not the sensitivity. Mechanically induced instabilities (e.g. changing mechanical intrinsic stress in the passivation layer system) of the sensor output also mainly affects the offset voltage.

3. Validation criteria

The validation of the stress test is divided into the following criteria for test group A and test group B:

- Test group A (thermo-electric stress):
  Long term stability parameters are within specified limits ($p_{pk} > 1.05$, chapter 4 and chapter 6)
- Test group B (thermo-mechanical stress):
  Offset shift for each stress load is less than 0.3% FS ($p_{pk} > 1.05$, chapter 4)

4. Test samples

The dies for both test groups are mounted in TDK’s standard housing.

The sample sizes for pressure dies are limited in particular by the test setup, the batch size per test and the test duration. Therefore, lower sample sizes as required in the AEC-Q101 pass criterion[2] are used under the following conditions:

- The measured values are available and not only pass/fail data.
- The measured distribution can be considered as a normal distribution according to statistical tests.

Robustness Validation

The AEC-Q101 pass criterion[2] is: "No failures in a 3*77=231 sample size". This is statistically equivalent to the fact that a failure rate in the global entity of 1% can be assumed with 90% confidence (or a rate of 0.4% with a confidence of 60%).

Using statistical distribution analysis, the AEC-Q101 pass criterion[2] can be translated to the following acceptance criterion: "The lower limit of the process capability p_{pk} confidence interval is bigger than 0.77 for the failure rate of the global entity of 1%. To achieve a 90% confidence interval for a sample size of 27 dies, the expected process capability p_{pk} is 1.03 and the upper p_{pk} level is 1.29." (For p = 0.4% the 90% confidence interval is $[p_{pkl}, p_{pku}] = [0.88, 1.14]$ with $p_{pk} = 1.01$ for a sample size of 27 dies)". Hence for the long-term stability parameter, the AEC-Q101 pass criterion[2] is always fulfilled if $p_{pk} > 1.05$.

In the Appendix, you will find statistical details and the evaluation of the AEC-Q101 pass criterion[2].

5. Qualification tests (see Table 1 and Figure 1)

The test samples are divided in two main test groups.

- Group A is testing failures, which occur by applying temperature loads under biased condition. Electronic effects in semiconductors could cause failures, like offset voltage drift due to mobile ions in silicon oxide.
- Group B is testing under temperature loads without bias to detect possible thermo-mechanical failures, like for instance signal drift due to annealing of process induced stresses or temperature hysteresis due to plastic deformations.

An additional test group D is assigned for burst pressure tests and testing the bond pad area by using a wire bonding process and a wire pull test.

Table 1 shows all tests performed in test groups A, B, and D. The "Reference" column lists all technical standards according to AECQ101[2]. Just the TCB test is based on TDK's internal standard. Only AEC Standard Q101 tests for bare dies are considered.

Figure 1 illustrates the test flow. From three wafers, in total 63 dies are assembled in standard TDK housings.

Thereof, two times 27 pressure sensors are used in the two test groups A and B for biased and unbiased tests. 27 additional dies are needed for the burst test, which are assembled therefore in a special burst test carrier. For the bond pad test, bond wires of 9 assembled dies are pulled (WBI) after high temperature storage (HTS). For dies with operating pressure > 6 bar additional 27 bare dies are put to the temperature cycle test (TC see Table 1), using a ceramic tray. After the TC test, the dies are assembled on burst test carrier and the burst pressure test is done to evaluate a thermo-mechanical impact of the TC test.

In total 90 dies for rated pressure < 6 bar and 117 dies for rated pressure > 6 are used – from each wafer 30 or 39 dies, respectively.

For the overpressure test, dies from group A or group B can be used, as the temperature loads of the two groups are similar. No impact of the bias to the overpressure is expected. Only for dies with a rated pressure < 6 bar, dies from group B have to be used for the overpressure test to verify that the overpressure does not affect the TC test.

Robustness Validation

Qualification test plan based on AEC-Q101

#	Abrv	Stress	Sample Size per lot	# of lots	Accept on # failed	Reference	Additional Requirements
	EV	External Visual	All qualification parts submitted for testing		0	JESD22 B-101	Inspect device construction, marking and workmanship.
	TEST	Pre- and Post-Stress Electrical Test	All qualification parts tested per the requirements of the appropriate device specification		0	User or Standard specification	Test is performed as specified in the applicable stress reference at room temperature.
A1	PV	Parametric Verification	27	3	0	User or Standard specification	Test all parameters according to user specification over the device temperature range to ensure specification compliance.
A2/B2	PC	Pre-conditioning	27	3	0	MIL-STD-883F Method 1008.2	Bake the devices for min 12 hours at minimum 150 °C.
A6	HTB	High Temperature Bias	9	3	0	JESD22 A-108	1000 hours at junction temperature TJ = 150 °C, or specified TJ (max) rating, with device maximum supply voltage specification. Can reduce duration to 500 hours through increasing TJ by 25 °C. TEST before and after HTB as a minimum.
A4	TCB	Temperature Cycling Bias	9	3	0	intern AS100001	10 temperature cycles between -40 °C and 150 °C, with normal supply voltage specification. TEST before and after TCB.
A8/B6	OP	Overpressure	9	3	0	ZVEI Guideline for PS Qualification	3 pressure cycles between 0 and max. specified pressure increased by factor acc. spec. TEST before and after OP.
B1	HTS	High Temperature Storage	9	3	0	JESD22 A-103	1000 hours at 150 °C or 500 hours at 175 °C for Grade 1. TEST before and after HTS as a minimum.
A3/B3	LTS	Low Temperature Storage	9	3	0	JESD22-A119	48 hours at -55 °C. TEST before and after LTS.
B5	TC	Temperature cycling	9	3	0	JESD22 A-104	1000 cycles (at ambient temperature TA = minimum range of -55 °C to maximum rated junction temperature, not to exceed 150 °C). Can reduce duration to 400 cycles using TA (max) = 25 °C over device maximum rated TJ by 25 °C. TEST before and after TC as a minimum.
B8	WBI	Wire Bond Integrity	10 bonds from a minimum of 5 devices		0	MIL-STD-750 Method 2037	wire pull/bond inspection after HTS on all wires from a maximum of 5 parts.
D2	BP	Burst Pressure	9	2	0	ZVEI Guideline for PS Qualification	

Table 1: List of qualification tests

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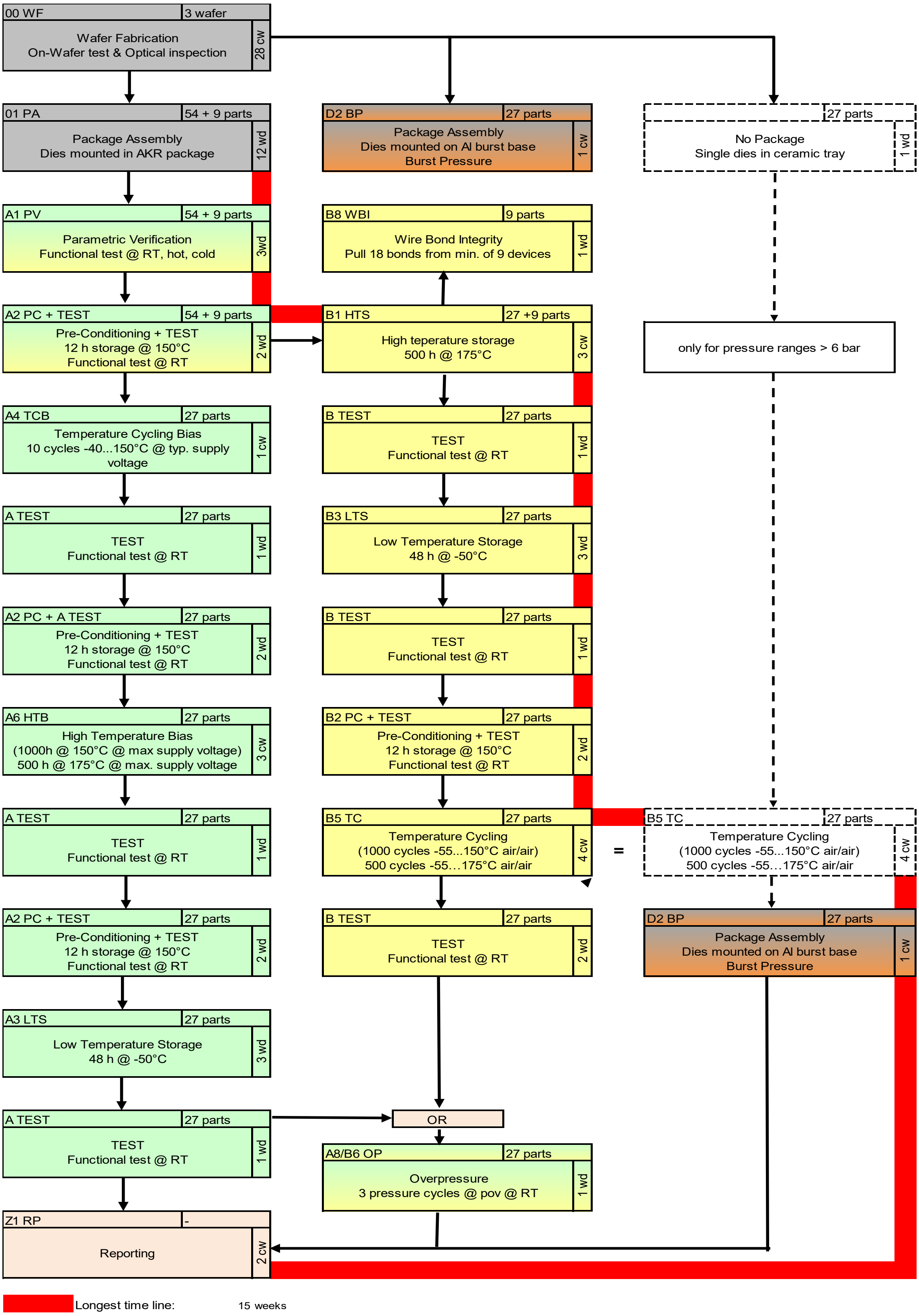

Figure 1: Qualification test flow

6. Long-term stability parameters

Remark: In this chapter, all voltages (unit mV/V or µV/V) and the sensitivity (unit mV/V/bar) are normalized to the bridge supply voltage $V_{DD.}$

6.1. Estimating the parameters $TCDV_0$ and THV_0 from the Temperature Cycle Bias Test (TCB)

The TCB test is performed to accelerate failure mechanisms which are thermally activated by the temperature cycle. Continuous measurement under bias conditions with a power supply voltage of 5 V determines both the mechanically and electronically induced instability of the sensor output.

Figure 3 shows the temperature cycle applied to estimate the temperature hysteresis THV_0 and temperature cycle drift $TCDV_0$ of the output voltage at atmospheric pressure for absolute pressure sensor dies or the offset voltage for gauge pressure sensor dies. Table 2 gives an overview of the measurement data and the conditions. The temperature is set by the temperature chamber. However, for each pressure sensor in the sample, the temperature is estimated using the bridge resistance R_b (T) as a function of temperature.

The temperature load regime starts with a holding temperature of 25 °C for 30 minutes. Then the temperature is increased to 150 °C at a temperature rate of 1 K/min. After the first 150 °C point 10 temperature cycles are performed between 150 and -40 °C at a temperature rate of 1 K/min. After the 11th temperature peak at 150 °C, the temperature is lowered to 25 °C and then held for 30 minutes. This holding temperature is referred to as the holding temperature after 150 °C of the 11th temperature cycle and is designated HT 150_{11}. Then an additional temperature cycle 25 °C, -40 °C, 25 °C is performed. The subsequent holding temperature of 25 °C for 30 minutes is referred to as the holding temperature after -40 °C of the 11th temperature cycle and is designated HT -40_{11}.

THV_0 is the difference of the corresponding normalized V_0 mean values to HT 150_{11} and HT -40_{11} in relation to the full-scale output span:

$$THV_0 = \frac{V_0(HT150_{11}) - V_0(HT - 40_{11})}{FSON} \; [\%FSON]$$

whereas FSON is the rated full scale normalized output span (units mV/V) as defined in the specification. In most cases FSON = 24 mV/V. The temperature hysteresis strongly depends on assembly conditions (gluing, material of mounting base). It is tested on samples assembled in standard TDK housings for design verification.

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To explain how to estimate the V_0 (HT 150_{11}) and V_0 (HT -40_{11}), see Figure 4, which shows details of the 25 °C, -40 °C, 25 °C temperature cycle with a holding temperature of 25 °C after 150 °C and after -40°C. The corresponding time interval for data selection to estimate V_0 (HT 150_{11}) or V_0 (HT -40_{11}) is defined by the temperature data acquisition interval. The temperature must be within the "**L**ower **L**evel **T**emperature of **D**ata **A**cquire **I**nterval" **LLTDAI** and the "**U**pper **L**evel **T**emperature of **D**ata **A**cquire **I**nterval" **ULDTAI** (LLTDAI < T_i < ULTDAI). For the estimation of the mean value of V_0 (T_i), only temperatures of T_i which lie between the "**L**ower **L**evel **T**emperature of **D**ata **S**ampling **I**nterval" **LLTDSI** and the "**U**pper **L**evel **T**emperature of **D**ata **S**ample **I**nterval" **ULDTSI** (LLTDSI < T_i < ULTDSI) are selected. The V_0 (HT 150_{11}) or V_0 (HT -40_{11}) are calculated as mean value of the corresponding selected V_0 (T_i).

To estimate $TCDV_0$ and the temperature hysteresis during the temperature cycle, the offset or the output voltages are sampled at a constant sample temperature using linear interpolation with two measured V_0 (T_1) and V_0 (T_2) at a temperature near T_s ($T_1 < T_s < T_2$). The corresponding output or offset voltages to the sampling points Sp (T_k) at T_s = 35 °C are assigned to V_0 (150_k) or V_0 (-40_k). Sp (-40_0) is the first sampling point after the initial holding temperature of 25 °C. V_0 (-40_0) at the sampling point Sp (-40_0) can be used as a reference point for estimating the deviation from V_0 DEV V_0 (T, #k):

$$DEV\ V_0(T,\#k) = V_0(150_k) - V_0(-40_0)$$

These values can be used for depicting the data in diagrams.

$TCDV_0$ is estimated from V_0 (150_{11}) and V_0 (150_1) (see Figure 3) using the equation:

$$TCDV_0 = \frac{V_0(150_{11}) - V_0(150_1)}{FSON}\ [\%FSON]$$

FSON is the rated full scale output span as defined in the specification.

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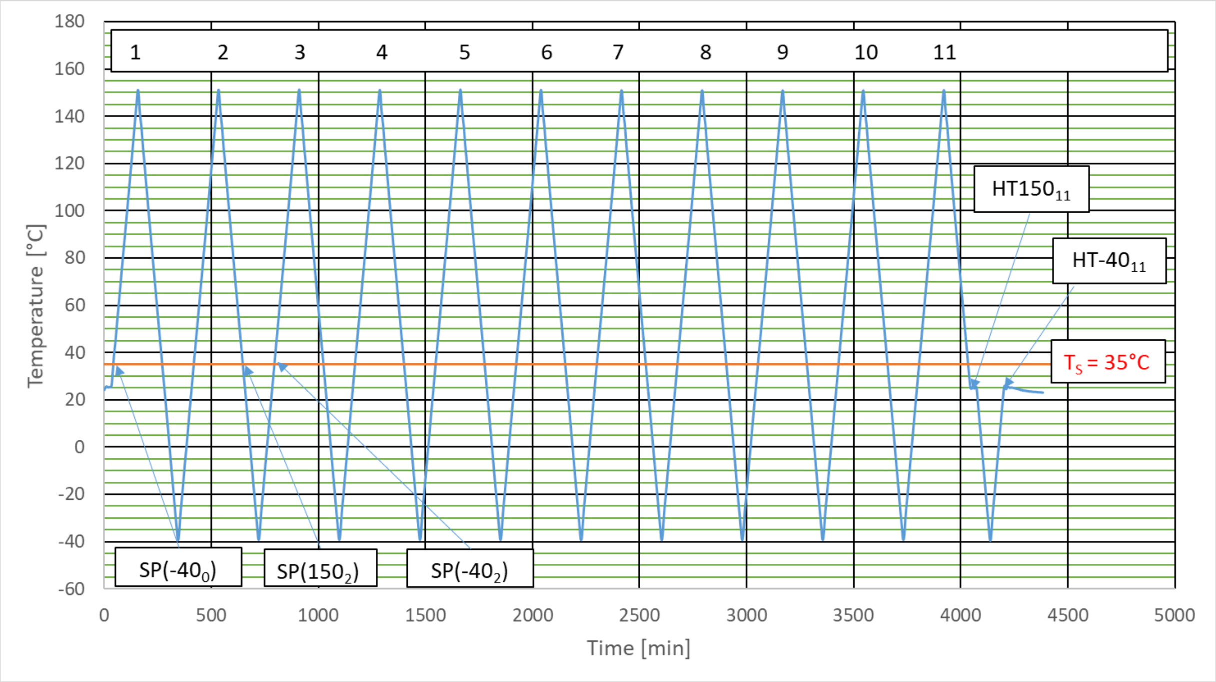

Figure 2: Temperature load of the temperature cycling bias test (TCB) with the definition of the V_0 data sampling points (Please refer to text for details.)

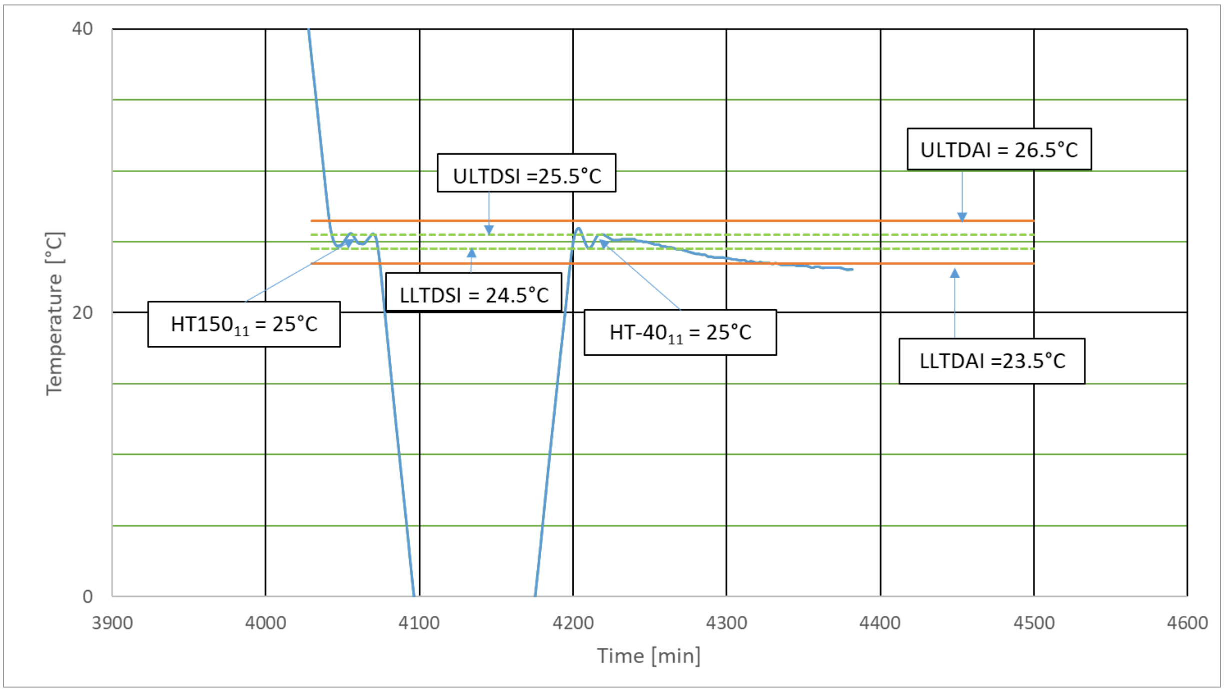

Figure 3: Details of the 11th temperature cycle 25 °C, -40 °C, 25 °C with a holding temperature of 25 °C after 150 °C and after 40° for assembling V_0 data for temperature offset voltage hysteresis THV_0.

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Description	Short term	Measurement value	Parameter	V_{DD}[V]
Measurement points	Sp (T_k)	V_0 (T_k)	T_s = 35 °C	5
Holding temperature after 150 °C	HT 150_{11}	Mean value estimation V_0 (HT 150_{11})	24.5 °C < HAT 150_{11} < 25.5 °C	5
Holding temperature after -40 °C	HT -40_{11}	Mean value estimation V_0 (HT -40_{11})	24.5 °C < HAT -40_{11} < 25.5 °C	5
Temperature rate			1/min	
Holding duration			30 min	

Table 4: Conditions for the TCB test and data collecting

To match the specification for gauge pressure sensor dies the following condition has to be fulfilled:

$$|TCDV_0| < specified\ value$$

For absolute pressure sensor dies the output voltage changed with the output pressure. To eliminate the impact on the atmospheric pressure on evaluation results, the mean value (MV) and the standard deviation σ of $TCDV_0$ of a sample of 27 dies are estimated. To meet the specification, the following conditions have to be fulfilled:

$$|TCDV_0 - MV| < specified\ value$$

$$3\sigma < specified\ value$$

The temperature drift of offset voltage depends strongly on assembly conditions (gluing, material of mounting base). It will be tested for design verification on samples mounted on AK2 transducer package (a reference data sheet for AK2 is available on the TDK website).

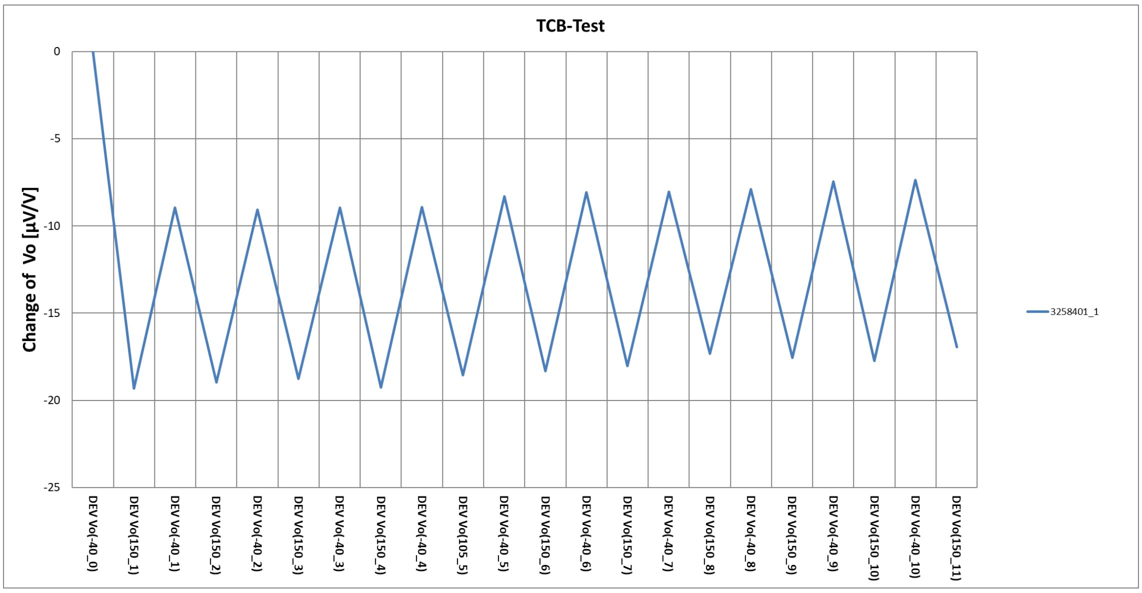

Figure 4: Example for a TCB test. DEV V (0) is assigned to the sampling point Sp (-40_0) at 35 °C after the initial hold temperature. It is the reference for the DEV V_0. $TCDV_0$ is calculated from DEV (150_{11}) and DEV (150_1).

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Figure 4 shows an example for a result of a TCB test. The $TCDV_0$ is calculated from DEV (150_{11}) and DEV (150_1) using:

$$TCDV_0 = \frac{DEV\ V_0(150_{11}) - DEV\ V_0(150_1)}{FSON} = \frac{-17\mu V/V + 19\mu V/V}{24000\mu V/V} = 0.01\%FSON$$

It is recognizable, that the temperature hysteresis after each temperature cycle is about -9 µV/V, which is in accordance to the temperature hysteresis of 8.3 µV/V, which was estimated from HT (150_{11}) and HT (-40_{11}). The temperature hysteresis difference due to the effect of the heat capacity and the thermal conductivity of the samples, as well the measurement set up by fast temperature ramping, can be eliminated successfully by using the bridge resistance as temperature sensor.

6.2 Estimating the parameters $HTDV_0$ from High Temperature Bias Test (HTB)

$HTDV_0$ is the high-temperature drift of offset voltage or output voltage V_0 at atmospheric pressure.

For the estimation of $HTDV_0$, a HTBM1-HTB-HTBM2-PC temperature load sequence is used, which is displayed in Figure 5 and stated in Table 6. V_0 values are measured at the sampling points m1, s1, s2, m2, m3, as stated in Table 7 which shows an overview of the data acquire regime for the estimation of $HTDV_0$.

The HTB test is a high temperature bias test with a temperature load of 150 °C for 480 h with a bias of 10 V. The output, respectively the offset voltage is not continuously scanned during the test. The output respectively the offset voltages are sampled every 30 s during the HTBM1 and HTBM2 phase. The time duration of the 150 °C temperature load is set to 10 h.

After the HTBM2 temperature load, samples are annealed at 150 °C (PC). In Figure 5 the PC temperature load is the pre-conditioning phase after the HTB test. The result of annealing can be used for root cause detection e.g. mobile ions in the oxide layer. If the signal drift after HTB is caused by mobile ions, the signal drift will decrease after PC phase. But if the signal drift is caused by a thermal mechanical effect, the signal drift will further increase after PC.

For estimating the high-temperature drift of offset voltage $HTDV_0$ use:

$$HTDV_0 = \frac{V_0(s_2) - V_0(s_1)}{FSON}\ [\%FSON]$$

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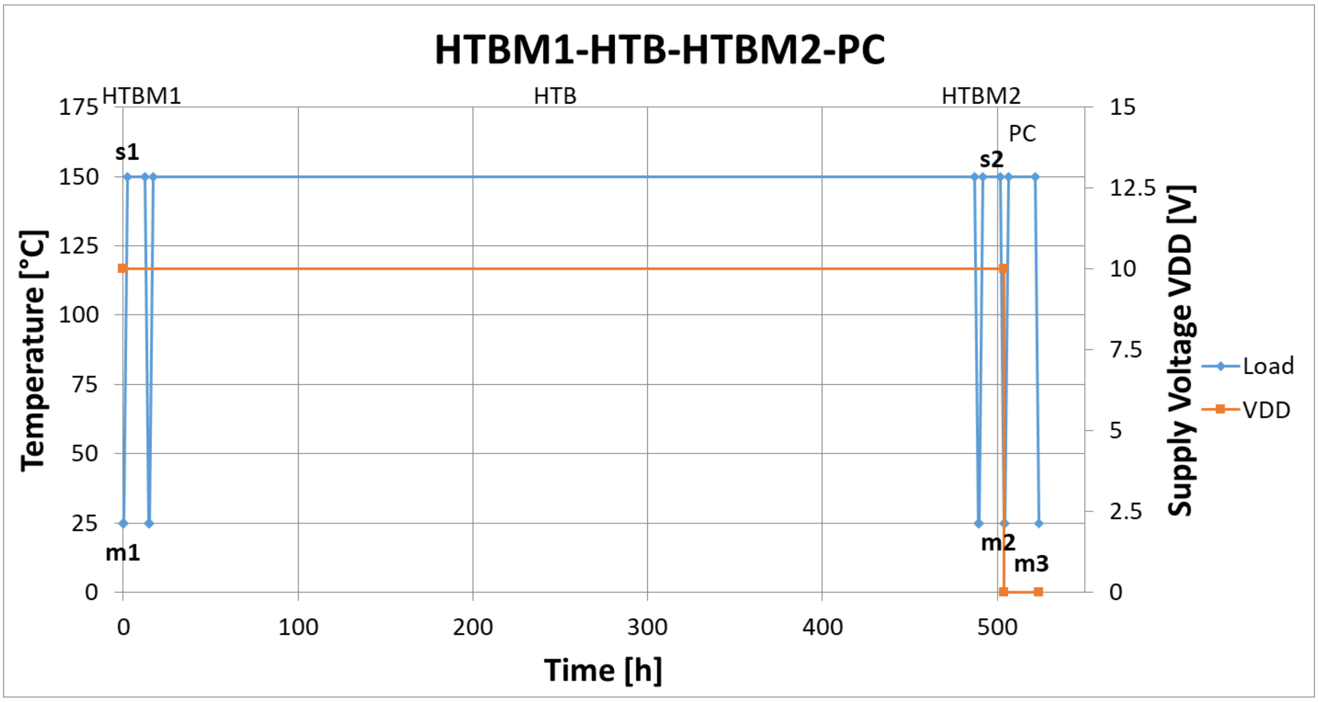

Figure 5: Load regime of the high-temperature bias related tests HTBM1, HTB, HTBM2, and PC

Description	T[°C]	V_{DD}[V]	Load Time[h]
HTBM1	150	10	10
HTB	150	10	480
HTBM2	150	10	10
PC	150	0	12

Table 6: Load regime of the high-temperature bias related tests HTBM1, HTB, HTBM2, and PC

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Measuring point	Data collecting	T [°C]	V_{DD}[V]	Time after load application
m1	TEST	25	5	before HTBM1
s1	Scan during HTBM1	150	10	3 h after start of HTBM1
s2	Scan during HTBM2	150	10	12 h after start of HTBM2
m2	TEST	25	5	after HTBM2
m3	TEST	25	5	after PC

Table 7: V_0 data acquire regime of the high-temperature bias related tests HTBM1, HTB, HTBM2, and PC.

In the specification FSON is defined as the normalized full scale output span, V_0 (s_1) and V_0 (s_2) as the normalized output voltage at atmospheric pressure for absolute pressure sensor dies or the offset voltage for gauge pressure sensor dies at the sampling points s_1 and s_2. To meet the specification for gauge pressure sensor dies the following condition has to be fulfilled:

$$|HTDV_0| < specified\ value$$

For absolute pressure sensor dies the output voltage changed with the output pressure. To eliminate the impact of the atmospheric pressure on evaluation results, the mean value (MV) and the standard deviation σ of $HTDV_0$ are estimated on samples. To meet the specification, the following conditions have to be fulfilled:

$$|HTDV_0 - MV| < specified\ value$$

$$3\sigma < specified\ value$$

Stated temperatures are the controlled temperatures of the test chamber environment. The test related junction temperature is approx. 25 K higher due to operation at power supply-voltage of 10 V, which cause a self-heating of the die.

6.3 Estimating the parameter $LTSV_0$

$LTSV_0$ is the Long-Term Stability of the output voltage.

To distinguish between the pre-conditioning phases after the tests we will assign the PC after the tests according to Table 8. In this table all tests are mentioned, which are used for estimating the $LTSV_0$ parameter. After each test the output characteristic, the offset voltage, the sensitivity, and the linearity are estimated at a constant temperature of (25 ±0.5) °C. This are the functional tests at 25 °C assigned as TEST in Figure 1.

Assign Figure 1	PC	TCB	PC	HTB	PC	LTS
Assign $LTSV_0$	PC_Start	TCB	PC_TCB	HTBM1, HTB; HTBM2	PC_HTB	LTS

Table 8: Assignment of the LTSV0 tests according to the list of qualification tests in Table 1 and Figure 1.

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$LTSV_0$ is a measure for the long-term stability of the offset voltage. It is estimated as the deviation of the offset voltage, measured after all tests as difference to the measurement after the PC_Start load. at (25 ±0.5) °C. (Remark: the PC_Start load is a thermal pre-conditioning of the samples). The parameter long-term stability of the offset voltage $LTSV_0$ is defined by the maximum value of all estimated deviations from V_0 (PC_Start):

$$LTSV_0 = MAX\left\{\left|\frac{V_0(after\ tests) - V_0(PC\_\_Start)}{FSON}\right| \quad \underset{Test\neq Start}{\forall} V_0(after\ tests)\right\}$$

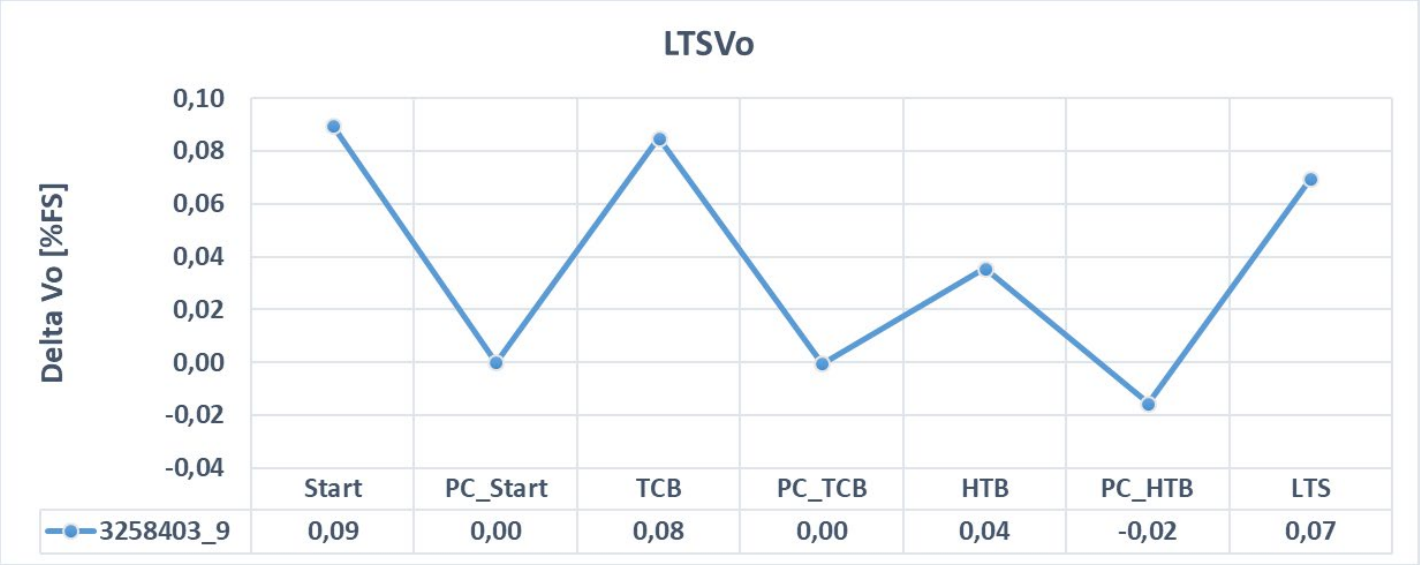
For absolute pressure sensing dies, the offset voltage is measured at 10% of the rated pressure. Hence $LTSV_0$ is defined by the maximum value of all estimated deviations from V_0 (PC_Start, $0.1p_r$):

$$LTSV_0 = MAX\left\{\left|\frac{V_0(after\ tests@0.1p_r) - V_0\left(PC\_\_Start@0.1p_r\right)}{FSON}\right| \quad \underset{Test\neq Start}{\forall} V_0(after\ tests@0.1p_r)\right\}$$

The start values V_0 (Start, 0.1 p_r) or V_0 (Start) respectively are excluded from the estimation of $LTSV_0$. FSON is referred as normalized value of an output span, which is defined in the specification. In most cases, this value is set to 24 mV/V, which is the common typical value of the output span at rated pressure. For an arbitrary output span the $LTSV_0$ (V_s) can be calculated by using:

$$LTSV_0[\%FS] = \frac{FSON}{V_s} LTSV_0[\%FSON]$$

with V_s as the arbitrary output span.



	Start	PC_Start	TCB	PC_TCB	HTB	PC_HTB	LTS
3258403_9	0,09	0,00	0,08	0,00	0,04	-0,02	0,07

Figure 8: Deviation Delta V_0 after each test for $LTSV_0$ evaluation. In the table below the diagram, the Delta V_0 value after each temperature cycle is noted.

Figure 8 shows an example for a LTSV$_0$ evaluation. After each test, the deviation delta V$_0$ value was estimated in relation of the reference point after the pre-conditioning temperature load PC_Start. After the TCB load, the temperature hysteresis can be detected, because the offset voltage hysteresis between PC_HTB and LTS is in the same range (0.09% FS). The Delta V$_0$ difference between HTB and PC_HTB is caused by mobile ions in the silicon oxide, but it is a very low value of < 0.06% FSON. According to the definition of LTSV$_0$ as the maximum of absolute values of the V$_0$ deviation after PC_Start, LTSV$_0$ is about 0.08% FSON.

7. Appendix: Statistical details to the AEC-Q101 pass criteria[2]

For a pass-fail test, the probability for finding a bad die in the sample population can be calculating using binominal statistic.

$$w(k) = \frac{n!}{(n-k)!\,k!} p^k (1-p)^{n-k}$$

$w(k)$ is the probability to find k bad dies within sample with a size of n dies. p is the failure rate in the global entity.

Samples size can be estimated by assuming a failure rate of 1% in the global entity, with a confidence level of 90%. If a failure rate of 1% in the global entity is assumed, the sample number have to be figured out, for which the probability is 10% to find no bad die or the probability is 90% to find any bad die in the sample.

Therefore, if the failure rate in the global entity is unknown and there is no bad die in the sample, it is allowed to conclude that the failure rate is smaller than 1% with a confidence level of 90%. With a similar argumentation it is possible to conclude, that the failure rate is smaller than 0.4% with a confidence level of 60%. To estimate the sample size for the above-mentioned conditions, the following equation for the sample size n has to be solved:

$$w(0) = (1-p)^n$$

For p = 1% and w(0) = 10% as well for p = 0.4% and w(0) = 40%, results a sample size of 230. If 3 lots are used, each lot should have a sub sample size of 77.

However, if a statistical distribution of measurement values is available, it is possible to approximate the mean value and the standard deviation. The mean value, the standard deviation and as well the process capability values c_{pk}, p_{pk} (X_{pk}) etc. are statistically distributed values. The X_{pk} confidence interval is a function of the X_{pk} value and the sample size. For a smaller sample size of 3 lots with each 9 samples per lot, the 90% p_{pk} confidence interval can be calculated.

Assuming for the long-term parameters LTX values e.g. $LTSV_0$ are in the range $0 \leq LT \leq LT_{UL}$; then the process capability p_{pk} is calculated by using:

$$p_{pk} = \frac{LT_{ULL} - \overline{LT}}{3\sigma}$$

with the mean value $\overline{LT}$, the specified upper level of the long-term parameter LT_{ULL} and σ as standard deviation of the normal long term parameter distribution. Therewith the limits of the confidence interval $[p_{pkl}, p_{pku}]$ are estimated by using[1]:

$$[p_{pkl}, p_{pku}] = \left[p_{pk} - z_{1-\frac{\alpha_c}{2}} \sqrt{\frac{1}{9N} + \frac{p_{pk}^2}{2(N-1)}},\ p_{pk} + z_{1-\frac{\alpha_c}{2}} \sqrt{\frac{1}{9N} + \frac{p_{pk}^2}{2(N-1)}} \right]$$

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whereas $z_{1-\frac{\alpha}{2}}$ is the percentile of the normal distribution at $1-\alpha_c/2$; α_C is defined by the confidence level $C = 90\%$ of the confidence interval:

$$\alpha_c = 1 - C$$

N is the number of the whole sample size.

To set up an equivalent for p = 1% with confidence level of 90% or p = 0.4% with confidence level of 60% for statistically distributed measurement values, the lower limit of the confidence interval p_{pkl} has to be calculated, assuming a normal distribution:

$$p_{pkl} = \frac{z_{1-p}}{3}$$

whereas z_{1-p} is the percentile of the normal distribution at $1-p$. This formula is valid assuming that the total probability below $2LT - LT_{UL}$ may be neglected. p_{pkl} is a function of p only and not a function of the sample size. However, the estimated X_{pk} values e. g. p_{pk} values are a function of the sample size. The value of p_{pk} is the higher value of 2 possible results of the equation:

$$p_{pkl} = p_{pk} - z_{1-\frac{\alpha_c}{2}}\sqrt{\frac{1}{9N} + \frac{p_{pk}^2}{2(N-1)}}$$

Failure Rate	p_{pkl}	Confidence	p_{pk}	p_{pku}
1,0%	0,775	90%	1,03	1,29
0,4%	0,884	60%	1,01	1,14

Table 9: Calculated lower, mean and upper value p_{pkl}, p_{pk}, p_{pku} of the process capability as function of failure rate and confidence for a sample size of 27 dies

Table 9 shows calculated values for the lower value of the process capability p_{pkl} for a failure rate of 1% or 0.4%, the expected process capability p_{pk} und the upper value of the process capability p_{ppu} for a confidence level of 90% or 60%, respectively.

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	Confidence Level 90%			Confidence Level 60%		
p_{pk}	p_{pkL}	p_{pku}	Confidence Range	p_{pkL}	p_{pku}	Confidence Range
0,5	0,34	0,66	0,31	0,42	0,58	0,16
0,6	0,43	0,77	0,35	0,51	0,69	0,18
0,7	0,51	0,89	0,38	0,60	0,80	0,20
0,8	0,59	1,01	0,42	0,69	0,91	0,22
0,9	0,67	1,13	0,46	0,78	1,02	0,24
1	0,75	1,25	0,50	0,87	1,13	0,26
1,1	0,83	1,37	0,54	0,96	1,24	0,28
1,2	0,91	1,49	0,59	1,05	1,35	0,30
1,3	0,99	1,61	0,63	1,14	1,46	0,32
1,4	1,06	1,74	0,67	1,23	1,57	0,34
1,5	1,14	1,86	0,72	1,32	1,68	0,37
1,6	1,22	1,98	0,76	1,41	1,79	0,39
1,7	1,30	2,10	0,80	1,49	1,91	0,41
1,8	1,38	2,22	0,85	1,58	2,02	0,43
1,9	1,45	2,35	0,89	1,67	2,13	0,46
2	1,53	2,47	0,94	1,76	2,24	0,48
2,1	1,61	2,59	0,98	1,85	2,35	0,50
2,2	1,69	2,71	1,03	1,94	2,46	0,52
2,3	1,76	2,84	1,07	2,03	2,57	0,55
2,4	1,84	2,96	1,12	2,11	2,69	0,57
2,5	1,92	3,08	1,16	2,20	2,80	0,59
2,6	2,00	3,20	1,20	2,29	2,91	0,62

Table 10: Calculated lower and upper level of the confidence interval [p_{pkl}, p_{pku}] and the confidential range of the process capability as function of the expected value of the process capability p_{pk} for a confidential level of 90% and 60%, respectively.

The lower level of the of the process capability p_{pkl} is increasing with p_{pk} because the derivative for all $p_{pk} > 0$.

$$\frac{dp_{pkl}}{dp_{pk}} > 0$$

Consequently, the AEC-Q101 criterion is fulfilled, if $p_{pk} > 1.05$. The failure rate at the lower limit of confidential interval at confidential level of 90 will decrease if the process capability will increase.

Table 10 shows the calculated lower and upper level of the confidence interval [p_{pkl}, p_{pku}] as well as the confidential range of the process capability as a function of the expected value for the process capability p_{pk} with a confidential level of 90% and 60% respectively. Finally, to ensure at least a $p_{pkl} = 1.33$, for a confidential level of 90% an expected value for the process capability $p_{pk} > 1.74$ or for a confidential level of 60% a $p_{pk} > 1.51$ is required. To ensure at least a process capability for $p_{pkl} = 1.67$ with a confidential level of 90% or 60%, an expected value of the process capability $p_{pk} > 2.18$ or respectively $p_{pk} > 1.9$ is needed.

References

[1] Minitap, Inc., “Minitap Help/Methods and Formulas/Process capability (Normal)/Confidence interval and bounds p_{pk},”, Minitap® 17.3.1, ©2013, 2016

[2] AEC - Q101 - Rev – D1 September 6, 2013

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