EPCOS Product Brief 2012

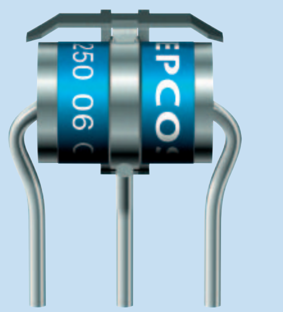
PSpice Model for Surge Arresters

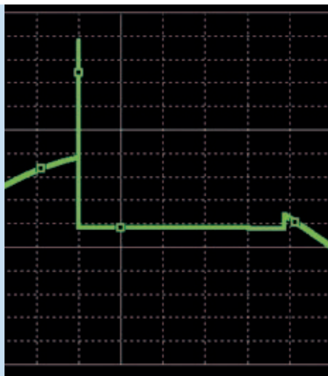
Analog Behavioral Model for Circuit Simulation

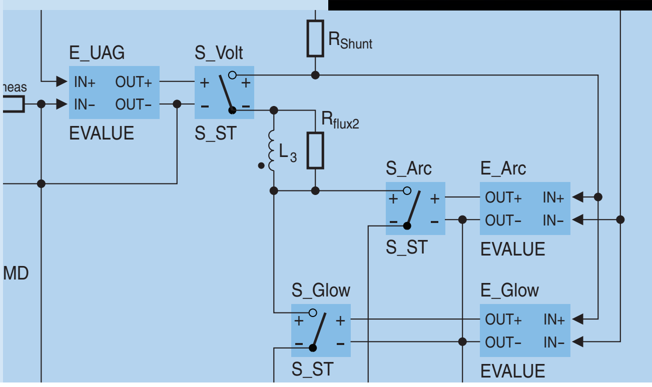
Voltage surges in telecom or power systems caused by lightning or line faults can affect sensitive electronic circuitry. Manufacturers of telecom equipment such as subscriber terminal boxes, DSL modems and power equipment or switched power supplies and UPS batteries are legally obliged to take overvoltage protection measures. Gas discharge tubes (GDTs) are typically used to shunt surge currents to ground and limit overvoltages to a harmless level. Their key advantages are their high surge current handling capability combined with a very low capacitance and high insulation resistance. EPCOS is the only manufacturer of surge arresters to offer simulation assistance and support for gas filled discharge tubes. Any arrester from the EPCOS product range can be entered into a PSpice model upon request. This allows users to fit the GDT into their designs at an early stage of development. Any effects occurring during normal operation as well as the behavior of the whole circuit under surge simulation can then be tested prior to building a prototype. This offers significant advantages such as cost savings and a reduced development time for new designs.

Applications

- Analog circuit simulation
- System design and verification
- Functional verification
- Surge simulation







PSpice Model for Surge Arresters

Simulation of gas discharge tubes

EPCOS provides network listings for specified arresters upon request. They are set up with ORCAD PSpice 16.3 and can be implemented in almost any Spice simulation program running basic libraries (such as ABM, ANALOG, BREAKOUT and SPECIAL). The very fast switching processes of arresters make the model highly CPU-intensive. When using fast transients (>0.1 kV/µs), the recommended step size for the simulation is 100 ns. Higher values may lead to deviating simulation results. The present design does not consider environmental factors such as heat dissipation and is purely ideal (excluding any variance). It is up to the user to determine the service life of the simulated arrester.

The model features the given values from the data sheet, including:

- DC spark-over voltage
- Impulse spark-over voltage
- Gap capacitance
- Insulation resistance
- Arc voltage
- Glow voltage
- Arc transition current
- Extinguishing current

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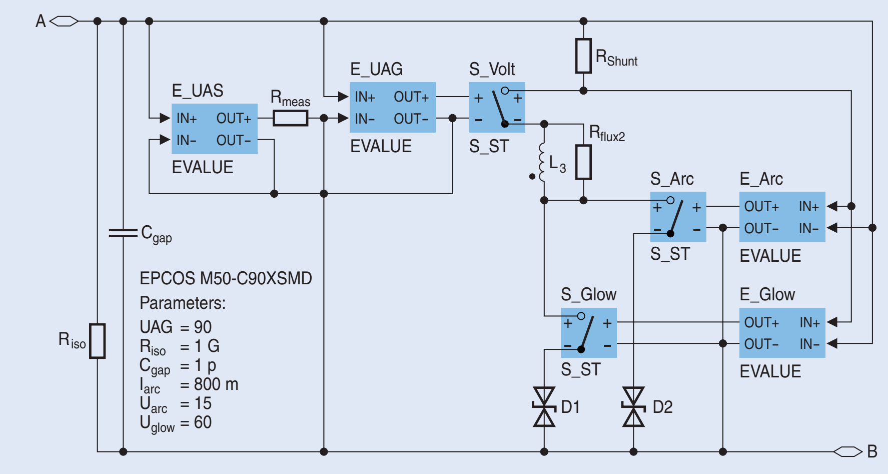
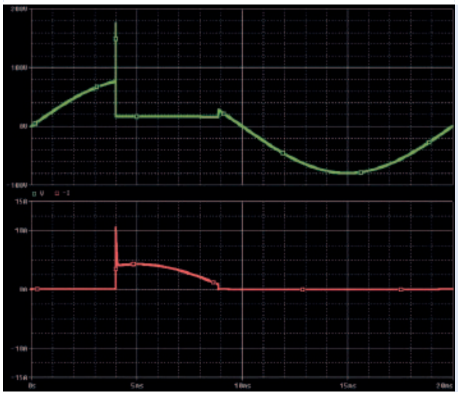
Circuit diagram of the simulation



This diagram shows a basic version of the arrester subcircuit in the PSpice model. The design can be fitted into a library file and used just like any other component in the editor.

Surge simulation



The diagram shows the simulation result of an EPCOS arrester with 90 V DC breakdown voltage. The arrester is placed line-to-ground with a simulated 80 V AC source. At the 4 ms mark, a surge (8/20 µs, 1 kV peak) is applied to the line (green graph at top). It can be seen that the arrester limits the overvoltage to ~180 V (the simulated impulse breakdown voltage). It then enters its arc mode (~20 V) and the surge current is shorted to ground (red graph at bottom). As soon as the follow current drops below a certain level, the arrester extinguishes and its internal resistance immediately returns to its initial very high value (9 ms mark).

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