Ceramic Capacitor Technology

CeraLink™ Opens New Dimensions in Power Electronics
Ceramic Capacitor Technology
PLZT – a highly flexible ceramic material class

Lead 82
\[ \text{Pb} \]
207.2

Lanthanum 57
\[ \text{La} \]
138.91

Zirconium 40
\[ \text{Zr} \]
91.224

Titanium 22
\[ \text{Ti} \]
47.867

Piezo actuators

Capacitors
CeraLink™ at a first glance
CeraLink™ at a first glance
New demands for DC link capacitors

Improvements in power density and efficiency were mainly driven by semiconductor technology in the last decade.

Example: principle block picture and size comparison of a motor inverter

“Today the package of a motor inverter is mainly driven by the size of the capacitor, the bus bars, the terminal box and the filter components.”

Source: Plikat, Mertens, Koch, Volkswagen AG, Corporate Research, 2013

Requirements for a DC link capacitor

- High capacitance density
- High current density
- Low parasitic values (ESR/ESL) for fast switching
- Low losses in operation
- High operating and peak temperatures
- High cooling efficiency due to high thermal conductivity
- Support of distributed DC link capacitor topologies with low inductance components (modular design)
Technology guideline

Film Capacitor
- more compact
- higher operating temperature
- lower ESL
- higher frequency
- SMD
- higher ripple current ratings

Large MLCC Chips
- more compact
- less footprint
- lower ESL
- more robust

Stacked MLCC
- higher cap-density at $V_{op}$
- higher operating temperature
- lower ESL
- higher ripple current ratings

CeraLink
- Standard semiconductor technology
- Enhanced technologies / modular ceramic designs possible / automotive
- High-end and high-temperature applications / fast switching (SiC) / full ceramic DC-link solutions
How does CeraLink™ meet these requirements?

Material

- High capacitance density
- Low losses
- Low parasitic values

Ceramic chip features

- High operating and peak temperatures
- High cooling efficiency
- High current density

Packaging

- Modular design
Material
PLZT – an antiferroelectric material

<table>
<thead>
<tr>
<th>Nature of electrical polarization</th>
<th>Material class</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronic, ionic</td>
<td>(Ba,Nd)TiO, typ. NP0, C0G</td>
<td>ε constant over electric field and temperature</td>
<td>ε &lt; 100</td>
</tr>
<tr>
<td>Permanent dipoles form ferroelectric domains</td>
<td>BaTiO$_3$ (BTO), typ. X7R</td>
<td>ε up to 10,000 is possible</td>
<td>ε decreases strongly with electrical field</td>
</tr>
<tr>
<td>Permanent dipoles form antiparallel zones</td>
<td>(Pb,La)(Zr,Ti)O$_3$ (PLZT)</td>
<td>ε increases with field</td>
<td>ε low at zero bias</td>
</tr>
</tbody>
</table>

P Dielectric polarization
E Electrical field strength
ε Permittivity
High capacitance density at operating condition

- Due to antiferroelectric behavior, the characteristics of CeraLink™ are strongly non-linear and optimized for conditions under operation in power electronics.
- Film capacitors and class 1 ceramics have a dielectric constant (nearly) independent on the electrical field. \((\varepsilon < 100)\)
- The permittivity of ferroelectric (e.g. X7R) MLCC capacitors is decreasing with electrical field.
- CeraLink™ features an increasing dielectric constant up to the operating voltage.
- At higher AC voltage (peaks), the material is able to provide even higher permittivities.

### DC bias characteristics at room temperature

<table>
<thead>
<tr>
<th>Electric field [V/µm]</th>
<th>Dielectric constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1,000</td>
</tr>
<tr>
<td>2</td>
<td>2,000</td>
</tr>
<tr>
<td>4</td>
<td>3,000</td>
</tr>
<tr>
<td>6</td>
<td>4,000</td>
</tr>
</tbody>
</table>

#### Nominal / rated capacitance

<table>
<thead>
<tr>
<th></th>
<th>Film capacitor</th>
<th>Class 2 MLCC</th>
<th>CeraLink™</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal / rated capacitance</td>
<td>100 %</td>
<td>100 %</td>
<td>100 %</td>
</tr>
<tr>
<td>No bias voltage 0.5 (V_{RMS})</td>
<td>100 %</td>
<td>100 %</td>
<td>35 %</td>
</tr>
<tr>
<td>DC link voltage 0.5 (V_{RMS})</td>
<td>100 %</td>
<td>35 %</td>
<td>60 %</td>
</tr>
<tr>
<td>DC link voltage 20 (V_{RMS})</td>
<td>100 %</td>
<td>35 %</td>
<td>100 %</td>
</tr>
</tbody>
</table>
CeraLink™ is ideal for fast switching

Device characteristics lead to a low inductive commutation loop

- High capacitance density of 2 to 5 µF/cm³
- Low self-inductance (ESL) of 2.5 to 4 nH
- High thermal robustness allows CeraLink™ to be placed very close to the semi-conductor with operation up to 150 °C permissible
- No limitation of dV/dt
Ceramic Chip Features
Design for robustness against ceramic cracks

MLSC design
- Series connection of two MLCC geometries in one component.
- MLSC design prevents short circuits caused by cracks from mechanical overstress

MFD design
- Chip is segmented in height to reduce piezoelectric stress between active and inactive area

Breakdown voltage measurement
Weibull – 95% CI

- Stress in corner area scales with height of chip

![Diagram showing multilayer series capacitor design and equivalent circuit of series capacitances with failure percentage over voltage, and Weibull distribution parameters.](image)
Ceramic chip design for high current capability and high thermal conductivity

Copper inner electrodes

- Co-firing of PLZT ceramic material together with Cu is difficult, but possible
- Cu – process is one core competence of the piezo mother factory in Deutschlandsberg, Austria

Cross section of the CeraLink™ multilayer chip consisting of appr. 80 dielectric ceramic layers
Packaging
Robust interconnection of metallic contacts

- Silver sinter connection between ceramic body and lead frame
- Outer contacts made of CIC (copper invar* copper), to combine high electrical and thermal conductivity with low coefficient of thermal expansion
- All materials are excellent thermal and electrical conductors (lowest thermal and electrical resistance)
- Silver layer prevents cracking of the ceramic in case of mechanical overstress or solder shock → open mode!

*Invar: 36Ni-Fe
Low losses at high temperatures and frequencies

**Comparison @ 1 V\text{AC}, 1 \text{kHz}, 400 V\text{DC}, 25 ^\circ C**

- **Dissipation factor\( \tan \delta \)**
  - CeraLink
  - BTO

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>0</th>
<th>50</th>
<th>100</th>
<th>150</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dissipation factor ( \tan \delta )</td>
<td>80</td>
<td>40</td>
<td>20</td>
<td>0</td>
</tr>
</tbody>
</table>

**Comparison @ 0.1 V\text{AC}, 0 V\text{DC}, 25 ^\circ C**

- **Equivalent series resistance [Ω]**

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>10^4</th>
<th>10^5</th>
<th>10^6</th>
<th>10^7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equivalent series resistance [Ω]</td>
<td>10^{-3}</td>
<td>10^{-2}</td>
<td>10^{-1}</td>
<td>10^{-0}</td>
</tr>
</tbody>
</table>

**Low dielectric loss at high temperatures**

**Minimal ESR due to low-loss copper electrodes and HF-suited backend**

BTO = barium titanate oxide = standard MLCC material
Low self-heating and high current capability

Due to low losses at high temperature and high frequency, CeraLink™ can carry more current under these conditions.

<table>
<thead>
<tr>
<th>Measurement condition</th>
<th>MKP film capacitor</th>
<th>BTO Class 2 MLCC</th>
<th>CeraLink™</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical capacitance density @ DC link voltage, 20 V_{RMS}, 25°C</td>
<td>0.7 µF/cm³</td>
<td>2.5 µF/cm³</td>
<td>4.9 µF/cm³</td>
</tr>
<tr>
<td>Typical current rating per capacitance @ 100 kHz, 105°C</td>
<td>&lt; 1 A/µF</td>
<td>&lt; 4.5 A/µF</td>
<td>12 A/µF</td>
</tr>
</tbody>
</table>

Comparison @ 400 V_{DC}, 105 °C, 200 kHz

Comparison @ 400 V_{DC}, 85 °C, 5 A_{rms}

Measurements were carried out without active cooling (no forced air flow, no heat sink).
Exceptional lifetime at high temperatures

Lifetime @ 200 °C three orders of magnitude higher than that of conventional ceramic capacitors
Lifetime at high temperatures – comparison of ceramic capacitors

CeraLink™ offers highest lifetime and capacitance density compared to conventional ceramic capacitors
Low leakage current at high temperatures

CeraLink™ shows stable and outstanding high isolation properties compared to all existing capacitor technologies

- low leakage current at elevated temperatures even above 150°C
- No thermal runaway observed for CeraLink™ ceramic material
Parallel capacitors
No thermal runaway

The capacitance characteristic and low ESR of CeraLink™ avoid a thermal runaway:

Higher temperature leads to:
- Lower capacitance
- Higher impedance
- Lowest current through the hottest capacitor

![Graph of large vs. small signal capacitance, bias = 400V](image)

**Green**: CeraLink™ small signal capacitance measurement (0.1 V_{rms}, 1 kHz)

**Black**: TDK Megacap 1µF 630V → measurement (0.1 V_{rms}, 1 kHz)
Ceramic Capacitor Technology • CeraLink™

CeraLink™ Product portfolio – modular design

Basic element (chip)
7.85 mm x 6.84 mm x 2.65 mm

500 V
(for 650 V semiconductors)

700 V
(for 900 V semiconductors)

900 V
(for 1300 V semiconductors)

LP  J-leads
LP
FA  (2-10 chips)
SP  (20 chips)

Released / To be released soon
# CeraLink™ product range

<table>
<thead>
<tr>
<th>Series</th>
<th>Designed for</th>
<th>Nominal capacitance / rated voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>650 V semiconductors</td>
<td>900 V semiconductors</td>
</tr>
<tr>
<td>Low Profile LP (L leads)</td>
<td>1 µF / 500 V</td>
<td>0.5 µF / 700 V</td>
</tr>
<tr>
<td>Low Profile LP (J leads)</td>
<td>1 µF / 500 V</td>
<td>0.5 µF / 700 V</td>
</tr>
<tr>
<td>Flex Assembly FA10</td>
<td>10 µF / 500 V</td>
<td>5 µF / 700 V</td>
</tr>
<tr>
<td>Flex Assembly FA2 / FA3</td>
<td>2/3 µF / 500 V Release 09/18</td>
<td>1/1.5 µF / 700 V Release 09/18</td>
</tr>
<tr>
<td>Solder Pin SP</td>
<td>20 µF / 500 V</td>
<td>10 µF / 700 V</td>
</tr>
</tbody>
</table>
## Comparison
### New FA10 vs. SP

<table>
<thead>
<tr>
<th></th>
<th>Solder Pin (SP)</th>
<th>Flex Assembly (FA10)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ceramic chip</strong></td>
<td>PLZT ceramic, MLSC design, copper inner electrodes, sputter layer</td>
<td>PLZT ceramic, MLSC design, copper inner electrodes, sputter layer</td>
</tr>
<tr>
<td><strong>Number of ceramic chips</strong></td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td><strong>Lead frame</strong></td>
<td>Cu meander structure / solder pin</td>
<td>CIC (copper-invar-copper) multilayer material, J-shaped connectors for each chip; SMD mounting technology</td>
</tr>
<tr>
<td><strong>Voltage rating</strong></td>
<td>500 / 700 / 900 V</td>
<td>500 / 700 / 900 V</td>
</tr>
<tr>
<td><strong>Nominal capacitance</strong></td>
<td>5 µF (900 V) – 20 µF (500 V)</td>
<td>2.5 µF (900 V) – 10 µF (500 V)</td>
</tr>
<tr>
<td><strong>Current rating</strong></td>
<td>24 A_{rms} (1.2 A_{rms} per chip; 900 V type)</td>
<td>32 A_{rms} (3.2 A_{rms} per chip; 900 V type)</td>
</tr>
<tr>
<td><strong>Mounting area</strong></td>
<td>726 mm² (square area; 36 mm² per chip)</td>
<td>213 mm² (21.3 mm² per chip)</td>
</tr>
<tr>
<td><strong>Zhermomechanical stability</strong></td>
<td>-50 / 150°C / 1000 cycles no damage, no degradation</td>
<td>-55 / 150 °C / 1.000 cycles no damage, no degradation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-55 / 150 °C / 10.000 cycles tested on the package system w.o. damage</td>
</tr>
<tr>
<td><strong>Weight per chip</strong></td>
<td>1.55 g</td>
<td>1.15 g</td>
</tr>
</tbody>
</table>
SiC market
Availability of various voltage classes

1200 V SiC power modules → Ideal for our 900 V series

Source: Littlefuse white paper
Application example - Industry
Integrated servo drive

Traditional design

Integrated servo drive

... electronics is integrated into the motor housing
... SiC for new designs

Temperature

Low ESL
Application example - Automotive Onboard chargers

Example

Recommended products (selection)

1. Chip NTCs (thermal sensing against overheating)
   - B57232V5103+360
   - B57332V5103+360
   - NTCG164LH104H

2. Chip varistors (ESD protection for data lines)
   - CT0402S17AG
   - CT0603L25HSG
   - AVRM1608C270MT*

3. Chip varistors (low voltage surge protection)
   - CT0805S14BAUTOG
   - CT1206S14BAUTOG
   - CT2220K30G
   - AVRM2012C390KT6AB

4. Ledged varistors (high voltage surge protection)
   - SNF14K***E2K1
   - SNF20K***E2K1

5. Surge arresters (high voltage protection)
   - EHV6*-H…B1-B7
   - EHV60-H…SMD

6. PTC ICLs (inrush current protection)
   - J21x series

7. CeraLink™ (DC link capacitor or output filtering)
   - B58031*
   - Flex Assembly FA2 or FA3
Application examples
Ideal for demanding applications

Motor sports
- Power supplies for medical equipment
- Test & measurement

Electric aircraft
- Down-hole power supplies (gas & oil)
- Traction (SiC)

Temperature
Robust Design
Low weight
Small size
Outlook:
Chip CeraLink™ 2220 in development

<table>
<thead>
<tr>
<th></th>
<th>TDK MLCC Height: 2.5 mm</th>
<th>CeraLink™ 2220 Height: 1.4 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance @ 0 V DC, 25 °C</td>
<td>470 nF</td>
<td>60 nF</td>
</tr>
<tr>
<td>Capacitance @ 400 V DC, 25 °C</td>
<td>183 nF</td>
<td>110 nF</td>
</tr>
<tr>
<td>Capacitance @ 400 V DC, large signal, 25 °C</td>
<td>183 nF</td>
<td>220 nF</td>
</tr>
<tr>
<td>Size [l x w x h]</td>
<td>5.7 x 5 x 2.5 mm</td>
<td>5.6 x 4.7 x 1.4 mm</td>
</tr>
<tr>
<td>Capacitance density @ 400 V DC (400 V DC large signal)</td>
<td>2.57 µF/cm³</td>
<td>3.4 (6.6) µF/cm³</td>
</tr>
<tr>
<td>T_{max}</td>
<td>125 °C</td>
<td>150 °C</td>
</tr>
<tr>
<td>I_{rms} @ 100 kHz*</td>
<td>2.1 A_{RMS}</td>
<td>4.0 A_{RMS}</td>
</tr>
</tbody>
</table>

* T_{amb} = 85°C / f = 100 kHz / VDC = 400V / calculated from I_{rms} = 3 A and device temperature after 15 min

Target: CeraLink™ 2220
2220 200 nF 500 V
Standard termination

Benchmark MLCC: C5750X7T2J474K250KC
2220 470 nF 630 V
Standard termination

- Optimized for capacitance density (MLCC design)
- No stress-relief layer necessary for 1 mm active packet (1.4 mm chip height)
- Termination: Cu cap with Ni/Sn galvanics
Summary

Key benefits of CeraLink™

● Effective capacitance increases with rising voltage and leads to **high capacitance density**

● **Low ESL** and low inductive connection

● **Low ESR** especially at high frequencies and high temperatures

● **High current density**

● **High operating and peak temperatures** with temperature excursions up to 150°C

● **High robustness against high temperatures**

● Supports **fast-switching semiconductors** and high switching frequencies

● Supports further **miniaturization** of power electronics at the system level