Ceramic capacitor technology

CeraLink® opens new dimensions in power electronics
CeraLink in a shot - optimized for conditions under operation in power electronics

Use CeraLink when
- Space requirement is tight
- Temperature is demanding (+150 °C)
- High current rating is vital
- Requirements for capacitance density are tough
- High switching frequencies are applied (SiC, GaN)

Main function in HV application
- Snubber capacitor
- Filter capacitor
- Flying capacitor
- DC-Link capacitor

CeraLink technology supports
- Increasing capacitance with DC bias and best in class capacitance density at operating point ($V_{op} + T_{op}$)
- High current capability due to low losses at high frequencies (up to several MHz) and high temperatures (up to +150 °C)
- No limitation of dV/dt
- Good self-regulating properties
- Qualification based on AEC-Q200 rev. D

![Diagram of function of capacitors in e.g. motor drives]

**Measurement condition**

<table>
<thead>
<tr>
<th></th>
<th>Film capacitor</th>
<th>MLCC class II</th>
<th>CeraLink</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Typical capacitance density</strong> @ DC link voltage, 20 $V_{RMS}$, 25 °C</td>
<td>0.7 µF/cm³</td>
<td>2.5 µF/cm³</td>
<td>4.9 µF/cm³</td>
</tr>
<tr>
<td><strong>Typical current rating per capacitance</strong> @ 100 kHz, 105 °C</td>
<td>&lt; 1 A/µF</td>
<td>&lt; 4.5 A/µF</td>
<td>11 A/µF</td>
</tr>
</tbody>
</table>
CeraLink’s special behaviour

Some differences to MLCC

<table>
<thead>
<tr>
<th>Linear</th>
<th>Ferroelectric</th>
<th>Antiferroelectric</th>
</tr>
</thead>
<tbody>
<tr>
<td>MLCC class I</td>
<td>MLCC class II</td>
<td>CeraLink</td>
</tr>
</tbody>
</table>

- Increasing capacitance with DC bias between 0 V and $V_{op}$
- Best in class capacitance density at operating point ($V_{op}$ & $T_{op}$)

Feature: Positive bias behaviour

More to this in the CeraLink Technical Guide
CeraLink’s special behaviour

At high temperature
- Operating temperature up to +150 °C
- Low losses at high temperature
- Low leakage current
- No thermal runaway
- Generally low self-heating AND self-heating supports CeraLink to come to temperature for good performance

At high frequency
- Optimal frequency in the range of 100 kHz to 1 MHz
- Minimal ESR due to low-loss copper electrodes and HF-suited backend
- Typ. ESR @ 25 °C, 1 MHz*: 3 … 45 mΩ
- Typ. ESL*: 2 … 4 nH
- No limitation of dV/dt
- Temperature decrease with rising frequency

Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions

<table>
<thead>
<tr>
<th>Measurement condition</th>
<th>MKP film capacitor</th>
<th>MLCC class II (BTO)</th>
<th>CeraLink</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical capacitance density</td>
<td>0.7 μF/cm³</td>
<td>2.5 μF/cm³</td>
<td>4.9 μF/cm³</td>
</tr>
<tr>
<td>@ DC link voltage, 20 V_RMS, 25 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Typical current rating per capacitance</td>
<td>&lt; 1 A/μF</td>
<td>&lt; 4.5 A/μF</td>
<td>11 A/μF</td>
</tr>
<tr>
<td>@ 100 kHz, 105 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*varies with series and voltage class
Technology Insights
Capacitor technology landscape

- Film capacitors
- MLCC class I
- MLCC class II
- Aluminum electrolytic capacitors
- EDLC
- CeraLink technology

Voltage vs. Capacitance graph showing the coverage of different capacitor technologies.
## Technology guideline

<table>
<thead>
<tr>
<th>Film capacitors</th>
<th>Large MLCC chips</th>
<th>Stacked MLCC</th>
<th>CeraLink</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Film capacitors" /></td>
<td><img src="image" alt="Large MLCC chips" /></td>
<td><img src="image" alt="Stacked MLCC" /></td>
<td><img src="image" alt="CeraLink" /></td>
</tr>
<tr>
<td>Smaller</td>
<td>Lower ESL</td>
<td>Smaller solution</td>
<td>Si IGBT</td>
</tr>
<tr>
<td>Higher operating temperature</td>
<td>Higher frequency</td>
<td>Higher operating temperature</td>
<td>SiC</td>
</tr>
<tr>
<td>Lower ESL</td>
<td>SMD</td>
<td>Lower ESL</td>
<td>GaN</td>
</tr>
<tr>
<td>Higher ripple current ratings</td>
<td></td>
<td>Higher ripple current ratings</td>
<td></td>
</tr>
</tbody>
</table>
Positioning CeraLink in capacitor landscape

### General Table

<table>
<thead>
<tr>
<th>Capacitance at voltage</th>
<th>Film capacitor</th>
<th>MLCC class II</th>
<th>CeraLink</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nom. / Rated capacitance</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>No bias voltage 0.5 V_RMS</td>
<td>100%</td>
<td>100%</td>
<td>35%</td>
</tr>
<tr>
<td>DC link voltage 0.5 V_RMS</td>
<td>100%</td>
<td>35%</td>
<td>60%</td>
</tr>
<tr>
<td>DC link voltage 20 V_RMS</td>
<td>100%</td>
<td>35%</td>
<td>100%</td>
</tr>
</tbody>
</table>

### Ceramic landscape

<table>
<thead>
<tr>
<th>Special requirements</th>
<th>MLCC class I</th>
<th>MLCC class II</th>
<th>CeraLink</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonance, stable C</td>
<td>✓</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>T &gt;125 °C</td>
<td>✓</td>
<td>X8R / custom</td>
<td>✓</td>
</tr>
<tr>
<td>V &gt;630 V</td>
<td>✓</td>
<td>Limited offer</td>
<td>✓</td>
</tr>
<tr>
<td>AC</td>
<td>✓</td>
<td>✓</td>
<td>×</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Consideration of total solution cost
CeraLink LP versus MLCC class II

Capacitance
@ 400 V + 20 V ripple

Similar like

Ripple current
@ 100 kHz & 85 °C

Similar like

Added value of CeraLink LP series

- Less PCB space
- Higher temperature
- Low ESL

Stacked MLCC based on case size 2220
CeraLink’s special behaviour… (1)

… positive bias behaviour

CeraLink features a non-linear capacitance behavior, i.e. the capacitance strongly depends on external parameters such as the applied DC bias voltage or the temperature. It is important to note that CeraLink is designed to have its capacitance maximum under operating conditions, i.e. under a DC bias (constant operating voltage) and with a superimposed ripple amplitude.

More to this in the CeraLink Technical Guide
CeraLink’s special behaviour… (2)

… at high temperatures

- Operating temperature up to +150 °C
- Low ESR
- Low leakage current
- No thermal runaway
- Superb heat transport capabilities to PCB due to copper-invar-copper (CIC) lead frames*
- High ripple currents of up to 11 A/μF
- Generally low self-heating AND self-heating supports CeraLink to come to temperature for good performance

*used for CeraLink® LP, FA and SP series
CeraLink’s special behaviour… (3)

... at high frequencies

- Perfect for frequencies up to 1 MHz
- No limitation of dV/dt
- Minimal ESR at high temperatures due to low-loss copper electrodes and HF suited backend
- Typ. ESL* 2 to 4 nH

➡ Perfect as snubber or in filter applications

*varies with series and voltage class
CeraLink product portfolio

<table>
<thead>
<tr>
<th>Series</th>
<th>Rated voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>500 V</td>
</tr>
<tr>
<td>Low profile</td>
<td></td>
</tr>
<tr>
<td>LP (L / J leads)</td>
<td>1 µF</td>
</tr>
<tr>
<td>Flex assembly</td>
<td></td>
</tr>
<tr>
<td>FA2 / FA3</td>
<td>2 / 3 µF</td>
</tr>
<tr>
<td>Flex assembly</td>
<td></td>
</tr>
<tr>
<td>FA10</td>
<td>10 µF</td>
</tr>
<tr>
<td>Solder pin</td>
<td></td>
</tr>
<tr>
<td>SP</td>
<td>20 µF</td>
</tr>
<tr>
<td>2220 series</td>
<td></td>
</tr>
<tr>
<td>SMD 2220 Standard + Soft Termination</td>
<td>0.25 µF @ h: 1.4 mm</td>
</tr>
</tbody>
</table>

Case size
SMD 2220

Basic element
7.85 x 6.84 x 2.65 mm

Released

500 V
700 V
900 V

LP
J leads

LP
L leads

FA
(2-10 chips)

SP
(20 chips)
CeraLink SMD 2220 series

- Optimized for capacitance density (MLCC design)
- Termination
  - Standard: Cu cap with Ni/Sn galvanics
  - Soft electrode: additional conductive resin layer absorbing mechanical stress

- 500 V component with 1.4 mm height
  - \( C_{\text{nom, typ}} \): 250 nF
  - \( I_{\text{RMS}} @100 \text{ kHz and } 85 \degree \text{C} \): 5 A
CeraLink product outlook

The chip size components

CeraLink SMD 2220 500 V
h: 1.4 mm
\( C_{\text{nom, typ}} \): 250 nF
Released

CeraLink SMD 2220
with maximum capacitance
due to higher height
500 V component
900 V component

CeraLink SMD 1210 500 V
with maximum capacitance
due to higher height
500 V component
900 V component

All case sizes in both termination available:
Cu cap with Ni/Sn galvanics, soft electrode with
additional conductive resin

... other voltage classes
Application Insights
CeraLink target applications

Main function
- Snubber capacitor
- Filter capacitor
- Flying capacitor
- DC-link capacitor

Scope
- High power density
- High efficiency
- High temperature

Principle circuit diagram of function of capacitors in e.g. motor drives

- EMC filtering
- AC/DC converter
- DC link
- DC/AC inverter
- Output filtering

- DC link
- Snubber
- Output filter

Output power [VA]
- Si IGBT
- GaN
- High power
- High speed
CeraLink®: Ideal for demanding applications (examples)

- **High-voltage applications in xEV**
- **Power supplies for medical equipment**
- **Test and measurement**
- **Drives**
- **Welding**
- **Traction (SiC)**

**Features**:
- Compact design
- Temperature
- High-voltage
- High current capability
- Low weight/low size
- Low ESL
- Robust design
## CeraLink as DC link

<table>
<thead>
<tr>
<th>Series</th>
<th>Maximum voltage ratings</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>650 V</td>
<td>1000 V</td>
</tr>
<tr>
<td>Flex Assembly FA10</td>
<td>10 µF / 500 V</td>
<td>5 µF / 700 V</td>
</tr>
<tr>
<td>Solder Pin SP</td>
<td>20 µF / 500 V</td>
<td>10 µF / 700 V</td>
</tr>
</tbody>
</table>

In parallel connection, higher temperature leads to:

- Lower capacitance
- Higher impedance
- Lowest current through the **hottest** capacitor → self-regulating properties
CeraLink as snubber
1 per half bridge - *mounted close to the semiconductor*

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<tr>
<td>Low Profile LP (L /J leads)</td>
<td>1 µF / 500 V</td>
<td>0.5 µF / 700 V</td>
</tr>
<tr>
<td>Flex Assembly FA2 / FA3</td>
<td>2/3 µF / 500 V</td>
<td>1/1.5 µF / 700 V</td>
</tr>
<tr>
<td>SMD SMD 2220 - New</td>
<td>0.25 µF / 500 V @ h: 1.4 mm</td>
<td>Coming soon in new h: 1.9 mm</td>
</tr>
</tbody>
</table>

Over-voltages or over-shoots occur when switching off a Semiconductor. This will cause an overvoltage according the formula (see left)
The low inductance of the CeraLink enables a faster switching of the semiconductor resulting in lower switching losses, enabling a reduction of switching losses of up to 40%!
CeraLink: Ideal for demanding applications

Key facts

Target applications

Automotive
- OBC
- DC/DC
- Auxiliary inverters for xEV (HV compressor, HV pump, HV heater)

Industry
- Drives
- Energy storage systems
- Power converter
- Solar inverters
- Power supplies like UPS, isolated power supply
- SiC Power Modules

- Suitable for HV designs like 400 V/800 V
- Increasing capacitance with DC bias and best in class capacitance density at operating point ($V_{op} + T_{op}$)
- Supports miniaturization with low inductive design

Basic facts

Qualification based on AECQ-200
Manufacturing site in EU (Deutschlandsberg, AT)
Quality management system according to IATF 16949:2016
Soldering Method: Reflow

Unique features

Innovative anti-ferroelectric ceramic material (positive bias behaviour)
High cooling efficiency due to high thermal conductivity
Good self-regulating properties

Resulting advantages

High capacitance density
High current capability
Low ESL (typ. 3 nH)
Low losses at high frequencies and high temperatures (up to +150 °C)
No limitation in dV/dt

→ Ideal as snubber, filter cap and flying capacitor for SiC and GaN applications