Ceramic Capacitor Technology

CeraLink® Opens New Dimensions in Power Electronics
CeraLink in a shot - optimized for conditions under operation in power electronics

Use CeraLink when
- Space requirement is tight
- Temperature is demanding (+150 °C)
- High current rating is vital
- Requirements for capacitance density are tough
- High switching frequencies are applied (SiC, GaN)

Main Application
- Snubber capacitor
- DC-Link capacitor
- Filter capacitor

CeraLink technology supports
- Increasing capacitance with DC bias and best in class capacitance density at operating point \( (V_{op} + T_{op}) \)
- High current capability due to low losses at high frequencies (up to several MHz) and high temperatures (up to +150 °C)
- No limitation of dV/dt
- Good self-regulating properties
- Qualification based on AEC-Q200 rev. D

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<th>Film capacitor</th>
<th>Class 2 MLCC</th>
<th>CeraLink</th>
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<td>&lt; 1 A/µF</td>
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CeraLinks Special Behaviour

At High Temperature
- Operating temperature up to +150 °C
- Low losses at high temperature
- Low leakage current
- No thermal runaway
- Generally low self-heating AND self-heating supports CeraLink to come to temperature for good performance

At High Frequency
- Optimal frequency in the range of 100 kHz to 1 MHz
- Minimal ESR due to low-loss copper electrodes and HF-suited backend
- Typ. ESR @ 25 °C, 1 MHz*: 3-45 mOhm
- Typ. ESL*: 2-4 nH
- Temperature decrease with rising frequency

Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions

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* varies with series and voltage class
Technology Insights
PZT – a highly flexible ceramic material class

Piezo actuators

Capacitors
CeraLink at a first glance

![Graph showing the comparison of CeraLink capacitors with other capacitor types such as Film capacitors, Ceramic capacitors, Aluminum electrolytic capacitors, and EDLC in terms of voltage and capacitance.](image)
Technology guideline

Film Capacitor

- more compact
- higher operating temperature
- lower ESL
- higher frequency
- SMD
- higher ripple current ratings

Standard semiconductor technology

Large MLCC Chips

- more compact
- less footprint
- lower ESL
- more robust

Standard semiconductor technology

Stacked MLCC

- higher cap-density at \( V_{op} \)
- higher operating temperature
- lower ESL
- higher ripple current ratings

Enhanced technologies / modular ceramic designs possible / automotive

CeraLink

High-end and high-temperature applications / fast switching (SiC) / full ceramic DC-link solutions
Material
PLZT – an antiferroelectric material

<table>
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<tr>
<th>Nature of electrical polarization</th>
<th>Material class</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronic, ionic</td>
<td>(Ba,Nd)TiO, typ. NP0, C0G</td>
<td>$\epsilon$ constant over electric field and temperature</td>
<td>$\epsilon$ &lt; 100</td>
</tr>
<tr>
<td>Permanent dipoles form ferroelectric domains</td>
<td>BaTiO$_3$ (BTO), typ. X7R</td>
<td>$\epsilon$ up to 10,000 is possible</td>
<td>$\epsilon$ decreases strongly with electrical field</td>
</tr>
<tr>
<td>Permanent dipoles form antiparallel zones</td>
<td>(Pb,La)(Zr,Ti)O$_3$ (PLZT)</td>
<td>$\epsilon$ increases with field</td>
<td>$\epsilon$ low at zero bias</td>
</tr>
</tbody>
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P Dielectric polarization
E Electrical field strength
$\epsilon$ Permittivity
High capacitance density at operating condition

- Due to antiferroelectric behavior, the characteristics of CeraLink are strongly non-linear and optimized for conditions under operation in power electronics
- Film capacitors and class 1 ceramics have a dielectric constant (nearly) independent on the electrical field ($\varepsilon < 100$)
- The permittivity of ferroelectric (e.g. X7R) MLCC capacitors is decreasing with electrical field
- CeraLink features an increasing dielectric constant up to the operating voltage
- At higher AC voltage (peaks), the material is able to provide even higher permittivities
CeraLink is ideal for fast switching

Device characteristics lead to a low inductive commutation loop

- High capacitance density of 2 to 5 \( \mu F/cm^3 \)
- Low self-inductance (ESL) of 2.5 to 4 nH
- High thermal robustness allows CeraLink to be placed very close to the semi-conductor with operation up to 150 °C permissible
- No limitation of dV/dt

![CeraLink schematic with semiconductor switching voltage and collector current](image)
New demands for DC link capacitors

Improvements in power density and efficiency were mainly driven by semiconductor technology in the last decade.

Example: principle block picture and size comparison of a motor inverter

“Today the package of a motor inverter is mainly driven by the size of the capacitor, the bus bars, the terminal box and the filter components.”

Source: Plikat, Mertens, Koch, Volkswagen AG, Corporate Research, 2013

Requirements for a DC link capacitor

- High capacitance density
- High current density
- Low parasitic values (ESR/ESL) for fast switching
- Low losses in operation
- High operating and peak temperatures
- High cooling efficiency due to high thermal conductivity
- Support of distributed DC link capacitor topologies with low inductance components (modular design)
Ceramic Chip Features
Design for robustness against ceramic cracks

MLSC design
- Series connection of two MLCC geometries in one component.
- MLSC design prevents short circuits caused by cracks from mechanical overstress

MFD design
- Chip is segmented in height to reduce piezoelectric stress between active and inactive area

Breakdown voltage measurement
Weibull – 95% CI

- Rated voltage 500 V
- Stress in corner area scales with height of chip

failure [%]
Voltage [V DC]
Packaging
Robust interconnection of metallic contacts

- Silver sinter connection between ceramic body and lead frame
- Outer contacts made of CIC (copper invar* copper), to combine high electrical and thermal conductivity with low coefficient of thermal expansion
- All materials are excellent thermal and electrical conductors (lowest thermal and electrical resistance)
- Silver layer prevents cracking of the ceramic in case of mechanical overstress or solder shock → open mode!

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*Invar: 36Ni-Fe
Low losses at high temperatures and frequencies

**Comparison @ 1 V\text{AC}, 1 kHz, 400 V\text{DC}, 25 °C**

- **Dissipation factor tan δ (10^{-3})**
  - CeraLink
  - BTO

- **Temperature (°C)**
  - 0 to 150

**Comparison @ 0.1 V\text{AC}, 0 V\text{DC}, 25 °C**

- **Equivalent series resistance [Ω]**
  - CeraLink 1μF
  - BTO MLCC 1μF

- **Frequency (Hz)**
  - 10^4 to 10^7

**Low dielectric loss at high temperatures**

**Minimal ESR due to low-loss copper electrodes and HF-suited backend**

BTO = barium titanate oxide = standard MLCC material
Low self-heating and high current capability

Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions.

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Comparison @ 400 V$_{\text{DC}}$, 105 °C, 200 kHz

Comparison @ 400 V$_{\text{DC}}$, 85 °C, 5 A$_{\text{rms}}$

Measurements were carried out without active cooling (no forced air flow, no heat sink)
Lifetime at high temperatures – comparison of ceramic capacitors

CeraLink offers highest lifetime and capacitance density compared to conventional ceramic capacitors.

Characteristic lifetime at 200 °C and 600 V

- **CeraLink** offers highest lifetime and capacitance density compared to conventional ceramic capacitors.

- **Class 2 MLCCs (BTO ceramic)**

A graph showing the characteristic lifetime at 200 °C and 600 V, with CeraLink offering the highest lifetime and capacitance density compared to class 2 MLCCs (BTO ceramic).
Low leakage current at high temperatures

CeraLink shows stable and outstanding high isolation properties compared to all existing capacitor technologies

- Low leakage current at elevated temperatures even above 150 °C
- No thermal runaway observed for CeraLink ceramic material

**Comparison @ 400 V\textsubscript{DC}**

![Comparison Graph](image)
CeraLink Product portfolio – modular design

Basic element (chip)
7.85 mm x 6.84 mm x 2.65 mm

500 V
(for 650 V semiconductors)

700 V
(for 900 V semiconductors)

900 V
(for 1200 V semiconductors)

LP
J leads

LP
L leads

FA
(2-10 chips)

SP
(20 chips)

Released
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<th>Maximum voltage ratings</th>
<th>Features</th>
</tr>
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<tr>
<td>Low Profile LP (L/J leads)</td>
<td>1 µF / 500 V</td>
<td>Innovative anti-ferroelectric ceramic material</td>
</tr>
<tr>
<td></td>
<td>0.5 µF / 700 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.25 µF / 900 V</td>
<td></td>
</tr>
<tr>
<td>Flex Assembly FA2 / FA3</td>
<td>2/3 µF / 500 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1/1.5 µF / 700 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.5/0.75 µF / 900 V</td>
<td></td>
</tr>
<tr>
<td>Flex Assembly FA10</td>
<td>10 µF / 500 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5 µF / 700 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5 µF / 900 V</td>
<td></td>
</tr>
<tr>
<td>Solder Pin SP</td>
<td>20 µF / 500 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 µF / 700 V</td>
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Use CeraLink when:
- Temperature is demanding (+150 °C)
- High current rating is vital
- Requirements for capacitance density are tough
- High switching frequencies are applied (SiC, GaN)

Qualified based on AEC-Q200 and Flex Assembly FA2/FA3.
Application Insights
Application examples
Ideal for Demanding Applications

High Voltage Application in xEV

Power Supplies for Medical Equipment

Test- & Measurement

Electric Flying

Down-hole Power Supplies (Mining)

Traction (SiC)

Temperature

High Voltage

High Current Capability

Compact Design

Low Weight Low Size

Low ESL

Robust Design
Application examples
Integrated servo drive

Traditional design

Electronics integrated into the motor housing (outside of inverter)
→ A lot of space
→ Separated from main temperature driver

Integrated servo drive

Electronics integrated into inverter box
→ Tight space requirements
→ Challenging temperatures
SiC based design
→ Low ESL requirements

Temperature

Low ESL
CeraLink inside Automotive ... some Success Stories

Target Application
• OBC
• DC/DC
• Auxiliary inverters
  • HV heater
  • HV pump
  • HV compressor

Often chosen due to
- Temperature
- Low Weight
- Low Size
- Low ESL
- Robust Design
### CeraLink as DC Link

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<th>Series</th>
<th>Maximum voltage ratings</th>
<th>Features</th>
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<tr>
<td></td>
<td>650 V</td>
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<td>FA10</td>
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<td>SP</td>
<td>20 µF / 500 V</td>
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In parallel connection, higher temperature leads to:

- Lower capacitance
- Higher impedance
- Lowest current through the **hottest** capacitor → self-regulating properties
CeraLink as Snubber
1 per half bridge - mounted close to the semiconductor

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| Low Profile LP (L /J leads) | 650 V: 1 µF / 500 V, 1000 V: 0.5 µF / 700 V, 1300 V: 0.25 µF / 900 V | • Low ESL (typ. 3 nH)  
  • Low losses at high frequencies and high temperatures (up to +150 °C)  
  • No limitation of dV/dt |
| Flex Assembly FA2 / FA3     | 650 V: 2/3 µF / 500 V, 1000 V: 1/1.5 µF / 700 V, 1300 V: 0.5/0.75 µF / 900 V |                                           |

Over-voltages or over-shoots occur when switching off a Semiconductor. This will cause an overvoltage according the formula (see left)
The low inductance of the CeraLink enables a faster switching of the semiconductor resulting in lower switching losses, enabling a reduction of switching losses of up to 40%!

\[ V = -L \cdot \frac{di}{dt} \]
CeraLink: Ideal Capacitors for Wide Bandgap Semiconductors

Target Application
- OBC
- DC/DC
- SiC Power Modules
- Auxiliary inverters for xEV (HV compressor, HV pump, HV heater)
- Wireless charging of vehicle

Suitable for designs of 400 V / 800 V xEV
- Increasing capacitance with DC bias and best in class capacitance density at operating point (Vop + Top)
- Supports miniaturization with low inductive design

Basic Facts
- Qualification based on AECQ-200
- Manufacturing site in EU (Deutschlandsberg, AT)
- Quality management system according to IATF 16949:2016
- Soldering Method: Reflow

Unique Feature
- Innovative anti-ferroelectric ceramic material
- High cooling efficiency due to high thermal conductivity
- Good self-regulating properties

Resulting Advantages
- High capacitance density
- High current capability
- Low ESL (typ. 3 nH)
- Low losses at high frequencies and high temperatures (up to +150 °C)
- No limitation in dV/dt

→ Ideal as snubber or filter cap for SiC and GaN applications
SiC based DC/DC Converter  
CeraLink as Snubber

Fast Power Electronics with Low Inductive Module Design

- DC/DC SiC power module: 2 phases - 800V, 100A, 130kHz each
- Ultra-low inductive commutation loop - inductance in low single-digit range realized with CeraLink LP 900 V 0.25 µF (B58031U9254M062)

Source: Hochschule Landshut
GaN power module with integrated driver and DC-Link capacitor

CeraLink as DC-Link capacitors

- Supports **miniaturization** with low inductive design
- Supports **fast-switching GaN** and high switching frequencies

- 1x CeraLink LP 500 V, 1 µF → low inductive commutation loop ~3nH
- 2x integrated driver for 2x GaN systems 650 V

Source: Fraunhofer IZM
## CeraLink Outlook

<table>
<thead>
<tr>
<th>CeraLink 2220 500 V 250 nF</th>
<th>Capacitance @ 0 V DC, 25 °C</th>
<th>70 nF</th>
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<tr>
<td></td>
<td>Capacitance @ 400 V DC, 25 °C</td>
<td>130 nF</td>
</tr>
<tr>
<td></td>
<td>Capacitance @ 400 V DC, large signal, 25 °C</td>
<td>250 nF</td>
</tr>
<tr>
<td></td>
<td>Size [l x w x h]</td>
<td>5.7 x 5.0 x 1.4 mm</td>
</tr>
<tr>
<td></td>
<td>Capacitance density @ 400 V DC (400 V DC large signal)</td>
<td>3.4 (6.6) µF/cm³</td>
</tr>
<tr>
<td></td>
<td>$T_{\text{max}}$</td>
<td>150 °C</td>
</tr>
<tr>
<td></td>
<td>$I_{\text{rms}}$ @ 100 kHz*</td>
<td>4.0 A_RMS</td>
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- Optimized for capacitance density (MLCC design)
- No stress-relief layer necessary for 1 mm active packet (1.4 mm chip height)
- Termination: Cu cap with Ni/Sn galvanics

* $T_{\text{amb}} = 85°C / f = 100$ kHz / VDC = 400V / calculated from $I_{\text{rms}} = 3$ A and device temperature after 15 min

And more… especially in the field of material development
Summary

Key benefits of CeraLink®

- Effective capacitance increases with rising voltage and leads to **high capacitance density**
- **Low ESL** and low inductive connection
- **Low ESR** especially at high frequencies and high temperatures
- **High current density**
- **High operating and peak temperatures** with temperature excursions up to 150 °C
- **High robustness against high temperatures**
- Supports **fast-switching semiconductors** and high switching frequencies
- Supports further **miniaturization** of power electronics at the system level