Product Brief 2024

AlN Multilayer Substrate Design Rules

Customized solutions for sustainable and high-power applications

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Wide bandgap (WBG) power semiconductors made from silicon carbide (SiC) and gallium nitride (GaN) are more and more deployed in applications like wind turbines, photovoltaic (PV) inverters, traction inverters for electric vehicles (EV), and EV fast chargers. Although these new semiconductors elevate the power density of these applications, they struggle with sufficient heat dissipation as power loss density also increases while chip sizes decrease.

TDK Electronics' new smart aluminum nitride (AlN) multilayer substrate pushes the boundaries of these wide bandgap semiconductors in terms of power density, reliability, and compact size. It is the key to more efficient EVs, lighter and more compact PV inverters, or significantly higher output power in an existing footprint.

TDK Electronics develops and customizes specific AlN packages and substrates for all high-power applications. It is a solution provider for smart multilayer substrates, bringing design to mass production.

Everything from a single source, manufactured in Europe. Tested, verified, and approved to the highest industry standards.

Figure 1: Complete panel size

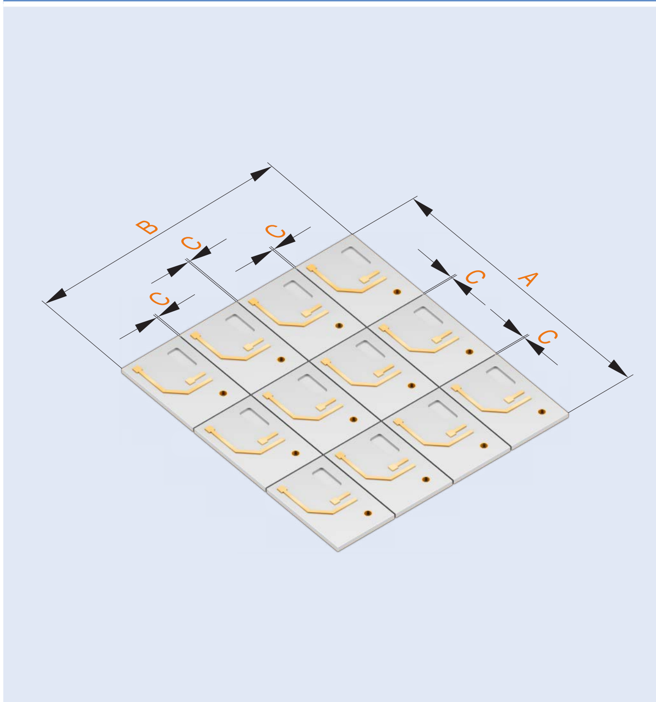

Figure 2: Critical package dimensions

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Feature	Parameter	Description	Dimensions	Reference
Panel	Panel length/width	Panel deliver size Region for customization	Max. 77 × 77 mm	A, B
	Module spacing	Gap between packages on panel	250 µm	C
AlN layers	Layer thickness	Thickness of individual AlN layers	30 & 100 µm[1]	D
	Cover layer thicknesses	Thickness of uppermost and lowermost AlN layer	Min. 100 µm	E
	Layer material	Ceramic material of layers	Aluminium Nitride (AlN)	
	Module thickness	Thickness range of package and panel	300 µm to 3 mm	F
W inner layers	Inner layer material	Material of inter layer electrodes	Tungsten (W)	
	Inner layer thickness	Thickness of W inner layers	5 µm to 15 µm[1]	G
	Inner layer spacing	Spacing of inner layers to package rim	500 µm	H
	Electrode spacing	Distance between different electrodes on same layer	Min. 50 µm ≥ 100 µm for pads ≥ 5 mm	I
	Electrode with	Width of W printed electrodes	Min. 60 µm[1]	J
Vias	Via size	Diameter of W vias	40 µm to 125 µm	K
	Via pitch	Distance between individual vias	Min. 1 via radius	L
	Via spacing	Spacing of vias to edge of electrodes	Min. 1 via radius	M
Cavity	Cavity depth	Depth of package cavities	Max. 500 µm	N
	Cavity spacing	Distance of gap towards package edge	1 mm (depending on the overall size of the cavity) $\frac{A_{cavity}}{A_{package}} << 1$	O
Power vias	Through holes/ Power vias holes	Diameter of through holes	2.5 mm[1]	P
	Through hole metallization	Metal on rim of through hole	Copper (Cu) Max. 150 µm	
Surface plating	Surface metal finishing	Type of metal on top and bottom side of package as well as inside cavities	ENIG/ENEPIG plating ENEPIG plating on Cu Selective finish possible	
	Plating thickness	Thickness of ENIPIG and Cu plating	ENEPIG: < 5 µm Cu: Max. 150 µm	Q
	Plating pitch	Distance between platings on surface	Min. 150 µm	R
	Plating spacing	Lateral distance between plating and package edge	Min. 250 µm	S

[1] Customized sizes possible on request

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